Passive Phase Shift Modulation for high-speed data transmission in implantable closed-loop neuroprostheses

By

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ABSTRACT

In designing a closed-loop implantable neuroprosthesis, naturally-occurring nerve signals will be used to control the stimulation. A telemetry system, capable of transmitting power to the implant and relaying two raw electroneurograms out of the body at high speed, yet having simple circuitry and working over a wide range of coupling coefficient with low power loss, is required. However, at the start of this project, no such device was available.

This thesis describes a novel method, *Passive Phase Shift Modulation* (PPSM), developed by the author, for high-speed passive reverse signalling via an inductively coupled link. A telemetry system based on PPSM is also devised by the author and presented in the thesis. In this system, power is provided to the implant and signals are conveyed out of the body continuously via the same radio-frequency (RF) channel. Unlike conventional *Passive Impedance Modulation*, it synchronously shorts the implant power-receiving coil for half the carrier cycle when a digital binary bit '1' is transmitted. This stores the energy in the coil and then releases it back to the circuit in time to generate a transient current surge in the transmitting coil, indicating a modulation. The scheme transmits phase shift modulation, but results in amplitude modulation.

The transient responses under PPSM have been explored in great depth by two approaches: 1) mathematically deducing the analytical solutions and 2) a semi-numerical method using modern computer aided tools. The results are comparable. The influence of the circuit parameters has been analysed, showing that the signal link does not disturb the optimised efficient power transfer link.

The telemetry system implementing PPSM is designed and built on the bench. It consists of a transmitter, an implant circuit, an external circuit and two coils. The digital logic is implemented by programmable gate arrays, bringing the electronic design up to date with modern technology. The performance is evaluated, and agrees with that predicted by theory and simulation.

PPSM has advantages in speed, energy efficiency, and simple circuitry with comparable working range compared to previous methods. It enables transmission of signals with large bandwidth without necessarily increasing the frequency of a carrier. It is, therefore, a satisfactory method for designing a practical feed-back controlled neuroprosthesis.

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ABBREVIATIONS, NOTATIONS and FORMULAE

ABBREVIATIONS

AM	Amplitude Modulation
CPLD	Complex Programmable Logic Device
ECG	Electrocardiogram
e.m.f.s	Electromagnetic fields
ESR	Effective Series Resistance
EMG	Electromyogram
ENG	Electroneurogram
FES	Functional neuromuscular electrical stimulation
FM	Frequency Modulation
IC	Integrated Circuit
ISI	Inter Symbol Interference
KVL	Kirchoff's voltage law
LARSI	Lumbar Anterior Root Stimulator Implant
N-FET	N channel Field-Effect Transistor
PM	Phase Modulation
RF	Radio Frequency
RFID	Radio Frequency Identification
SCI	Spinal Cord Injury
VHDL	VHSIC Hardware Description Language, (VHSIC is an abbreviation for Very High Speed Integrated Circuit).

NOTATIONS

A	Voltage gain across the inductive link $A = V_{C2}/E$
A_{max}	Maximal A
A1, A2, A3	Coefficients in the expression of $i_1(t)$ (in Appendix 5)
A_n (n = 1, 2, 3, 4)	Constants (in Appendix 7)
B1, B2, B3	Coefficients in the expression of $i_2(t)$ (in Appendix 5)
B_n (n = 1, 2, 3, 4)	Constants (in Appendix 7)
C	Capacitance

C_1	Transmitter tuning capacitance
C_2	Receiver tuning capacitance
C_3	Smoothing capacitance in the implant
C_{mod}	Modulating capacitance in *Passive Capacitive Modulation*
C_n (n = 1, 2, 3, 4)	Constants (in Appendix 7)
D	Rectifier diode in the implant
E	Amplitude of source voltage
f_0	Frequency of voltage source, or operating frequency.
f_1	Undamped frequency of the primary circuit when it is alone, corresponding to Ω_1.
f_2	Undamped frequency of the secondary circuit when it is alone, corresponding to Ω_2.
f_{d1}	Damped frequency of the primary circuit when it is alone, corresponding to ω_1.
f_{d2}	Damped frequency of the secondary circuit when it is alone, corresponding to ω_2.
f_d', f_d''	Damped frequency of the coupled circuit, corresponding to ω', ω''
g_1, g_1^*, g_2, g_2^*	Residues (in Appendix 5)
$\lvert g_1 \rvert$, $\lvert g_2 \rvert$	Amplitude of g_1, g_2 (in Appendix 5)
$\angle g_1$ and $\angle g_2$	Phase angles g_1, g_2 (in Appendix 5)
I_1, I_2, and I_3	Phasor currents
$I_1(s)$, $I_2(s)$, $I_3(s)$	Laplace transform of $i_1(t)$, $i_2(t)$, $i_3(t)$ respectively
i_1	AC current in the primary circuit
I_{1max}	Amplitude of the primary current
$\angle I_1$	Phase angle of the primary current
i_2	AC current in the secondary circuit
I_{2max}	Amplitude of the secondary current
$\angle I_2$	Phase angle of the secondary current
i_{1by_vc1}	Response of $i_1(t)$ resulting from initial condition $v_{C1}(t_{-1})$ (in Appendix 5)
i_{1by_vs}	Response of $i_1(t)$ resulting from input $v_s(t)$ (in Appendix 5)
$i_{2input}(t_0)$	The input responsible for generating $i_{1natural}$ in stage 3, $i_{2input}(t_0) = 2 \times i_2(t_0)$
$i_2(t_0)_{non\text{-}modulation}$	i_2 value at $t = t_0$ if there were no switching action

$i_{1transient}$	Transient current response in the primary circuit, $i_{1transient} = i_{1steady} + i_{1natural}$
$i_{1natural}$	Natural current response in the primary circuit
$i_{1steady}$	Steady current response in the primary circuit
k	Coupling coefficient
L	Inductance
L_1	Inductance of the transmitter coil (primary coil)
L_2	Inductance of the receiver coil (secondary coil)
M	Mutual inductance, $M = k\sqrt{L_1 L_2}$
m	Modulation index, m = $\frac{A-B}{A+B}$, where A is the signal maximum amplitude, and B is the signal minimal amplitude. In this thesis, B refers to amplitude without modulation
P	Power
P_1	Power dissipated in R_L
P_2	Power dissipated in R_{eq}
Q	Quality factor in general
Q_1	Quality factor of the transmitter circuit, $Q_1 = \frac{\Omega_1 L_1}{R_1}$
Q_2	Quality factor of the receiver circuit, $Q_2 = \Omega_2 R_2 C_2$
$\|r'\|$, $\|r''\|$	Amplitudes of the two damped cosine waveforms which compose $i_{1natural}$.
r', r'^*	Conjugate pairs of residues, $r' = \|r'\| e^{j\theta'}$, $r'^* = \|r'\| e^{-j\theta'}$ (Chapter 4 and 5)
r'', r''^*	Conjugate pairs of residues, $r'' = \|r''\| e^{j\theta''}$, $r''^* = \|r''\| e^{-j\theta''}$ (Chapter 4 and 5)
R	Resistance
R_0	Output resistance of the power transmitter
R_t	Series loss resistance of the transmitter coil
R_1	Sum of transmitter resistance, $R_1 = R_0 + R_t$
R_2	Sum of receiver resistance, $R_2 = R_r // R_{eq}$.
R_r	Parallel loss resistance of the receiver coil
R_t	Serial loss resistance of the transmitter coil
R_L	DC load representing the implant electronics
R_{eq}	Equivalent AC load to summarise D, C_3 and R_L,, $R_{eq} = ½ R_L$.
R_{on}	The resistance when the switch turns on

$R_{off.}$	The resistance when the switch turns off
R_{mod}	Modulating resistance in the *passive ohmic load modulation*
R_{sum}	Sum of the inductor (L_2) resistance and the switch resistance during the switch closing period
s	Laplace transform operator
s_n (n = 1, 2, 3, 4)	Roots (in Appendix 7)
T_0	A period of one RF cycle, $T_0 = \frac{2\pi}{\Omega}$
$T_e = 5/\alpha$	Duration of the exponential waveform $e^{-\alpha t}$ (Chapter 5)
$T_{sine1} = \frac{4\pi}{\omega' - \omega''}$	Period of the first sine wave in Eq. 5.10
$T_{sine2} = \frac{4\pi}{\omega' + \omega''}$	Period of the second sine wave in Eq. 5.10
$v_{C1}(t_0)_{non\text{-}modulation}$	v_{C1} value at $t = t_0$ if there were no switching action
V_{DC}	DC voltage on R_L
V_{C2rms}	Root-mean-square value of v_{C2}.
v_s	Source voltage (power transmitter output signal)
$V_s(s)$	Laplace transformation of $v_s(t)$
$\angle V_s$	Phase angle of v_s
v_{C1}	AC voltage on C_1
V_{C1max}	Amplitude of v_{C1}
$\angle V_{C1}$	Phase angle of v_{C1}
v_{C2}	AC voltage on C_2.
V_{C2max}	Amplitude of v_{C2}
$\angle V_{C2}$	Phase angle of v_{C2}
Z_2	Impedance of the secondary circuit
Z_{total}	Total impedance in a circuit equivalent to the coupled circuits
α_1	Damping constant of the primary circuit if it is alone, $a_1 = \frac{R_1}{2L_1}$ or $\alpha_1 = \frac{\Omega_1}{2Q_1}$
α_2	Damping constant of the secondary circuit if it is alone, $a_2 = \frac{1}{2R_2C_2}$ or $a_2 = \frac{\Omega_2}{2Q_2}$

α_T	Damping constant when the primary circuit couples to a terminal-shorted inductor.
α', α''	Damping constant of the coupled circuits
$1/\alpha_1$	Time constant of the primary circuit
$1/\alpha_2$	Time constant of the secondary circuit
$1/\alpha'$, $1/\alpha''$	Time constant of the coupled circuits
$\eta_{overall}$	Overall power transfer efficiency
η_{link}	Link efficiency
$\eta_{receiver}$	receiver efficiency
$\varphi 2$, $\varphi 3$	Phase angles (in Appendix 5)
θ', θ''	Phases of the two damped cosine waveforms which composed $i_{1natural}$.
τ	The switch closure duration
τ'	The duration of which the modulation, $\tau' > \tau$
Ω	Angular frequency of the voltage source corresponding to f_0
Ω_1	Undamped angular frequency of the primary circuit if it is alone, $\Omega_1 = \frac{1}{\sqrt{L_1 C_1}}$
Ω_2	Undamped angular frequency of the secondary circuit if it is alone, $\Omega_2 = \frac{1}{\sqrt{L_2 C_2}}$
Ω', Ω''	Undamped angular frequencies of the coupled circuits
ω_1	Damped angular frequency of the primary circuit if it is alone
ω_2	Damped angular frequency of the secondary circuit if it is alone
ω_T	Damped angular frequency when the primary circuit couples to a terminal-shorted inductor.
ω', ω''	Damped angular frequencies of the coupled circuits

FREQUENTLY USED FORMULAE

$$\Omega_1 = \frac{1}{\sqrt{L_1 C_1}} \qquad \Omega_2 = \frac{1}{\sqrt{L_2 C_2}}$$

$$f_1 = \Omega_1 / 2\pi \qquad f_2 = \Omega_2 / 2\pi$$

$$Q_1 = \frac{\Omega L_1}{R_1} \qquad Q_2 = R_2 C_2 \Omega$$

$$\alpha_1 = \frac{R_1}{2L_1} \qquad \alpha_2 = \frac{1}{2R_2 C_2}$$

or

$$1/\alpha_1 = 2Q_1/\Omega \qquad 1/\alpha_2 = 2Q_2/\Omega$$

$$\omega_1^2 = \Omega_1^2 - \alpha_1^2 \qquad \omega_2^2 = \Omega_2^2 - \alpha_2^2$$

or

$$\omega_1 = \frac{1}{2\pi}\sqrt{\Omega^2 - (\frac{\Omega}{2Q_1})^2} \qquad \omega_2 = \frac{1}{2\pi}\sqrt{\Omega^2 - (\frac{\Omega}{2Q_2})^2}$$

$$k = \frac{M}{\sqrt{L_1 L_2}}$$

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Part 1

Introduction and Objectives

Chapter 1 Introduction and objectives

1.1 Functional neuromuscular stimulation by feedback control

Functional neuromuscular electrical stimulation (FES) activates paralysed muscles or their nerves by electrical impulses to generate functional muscle movement. Neuroprostheses by FES have enabled patients with spinal cord injury (SCI) or brain damage to use their hands to pick up an object, to stand, walk and cycle with their own legs; to control bladder emptying; or to breathe [9, 39, 78, 79, 82, 85, 86]. However, most FES systems are either open-looped or have only limited feedback. In open-looped systems, the level of muscle activities needs to be closely monitored by the users or the researchers in order to recognize emerging problems; muscles are also often over-stimulated in order to secure adequate force, leading to premature fatigue, *etc.* [55]. The focus in FES research in recent years has been improving control by feedback. In particular, utilising natural electroneurograms (ENG) as control signals is advocated [52, 55, 88] and progress has been made to the point that some studies are ready to move from laboratories to further clinical investigations.

One such study, conducted at Aalborg university, is controlling hand grasp force. The researchers extracted the ENG, which is related to slippage events from a branch of the palmar digital nerve, and used it to adjust the electrical stimulation of forearm muscles, allowing a quadriplegic patient to hold an object with stability [48, 57].

Another example, also investigated by Aalborg university, is foot drop correction. The researchers detected the contact signal between skin and ground from the sural nerve, derived control timing from this information, then applied the electrical stimulation to the peroneal nerve in time with the swing phase of the leg and prevented foot drop. By this method, the external heel switch used in some existing systems is eliminated. Patients need not wear special shoes in order to walk faster and securely [45, 103].

Due to neurological damage to the pathways which control the bladder reflex, a patient with SCI often suffers from an overactive bladder. Bladder and urethra neck contractions no longer co-ordinate properly, resulting in urine storage and voiding

dysfunction. In many cases, the bladder and the urethra neck contract simultaneously. The frequent simultaneous contractions cause high bladder pressure and urine leakage, or even life-threatening kidney failure. Existing treatments to suppress bladder activity are taking drugs, cutting the sacral sensory nerve roots [5-8, 10], or delivering continuous stimulation via wire electrodes inserted in the sacral foramina[1]. However, these treatments either have side effects or involve a destructive procedure (cutting nerves). Recent research has demonstrated that the ENG signals, which are picked up by the cuff electrodes placed on the sacral nerve roots, increase in amplitude as the bladder contracts [40, 44, 61, 90]. If using these signals triggers a low level stimulation on the relevant sensory nerves, the bladder contraction can be inhibited [11, 61-63]. Combining the treatment with the sacral motor root stimulation for bladder emptying, an effective treatment of neurogenic incontinence is possible without the need for cutting the nerves, medication, or catheterisation [41, 59]. The life quality of patients with SCI thus could be greatly improved.

However, for such applications to be ultimately beneficial to patients, a practical feedback controlled implantable neuroprosthesis must be realised. Fig. 1.1 illustrates such a system. It consists of an implant device and an external unit. The implant power is supplied from the external side by an inductive coupling via a radio frequency (RF) signal. The RF received by the implant antenna is rectified and regulated to give a DC voltage. At the implant side, the raw ENGs picked up by the nerve electrodes are amplified and transmitted via a single radio carrier to the external side by a telemetry unit. A signal receiver at the external side recovers the ENGs. According to the ENG information, a Command & Control unit generates corresponding stimulation parameters which then modulate the RF of the power channel, sending the control signals forward to the implant, to trigger the stimulation.

[1] Medtronic Intersim stimulator Medtronic, Inc. Minneapolis, MN, USA

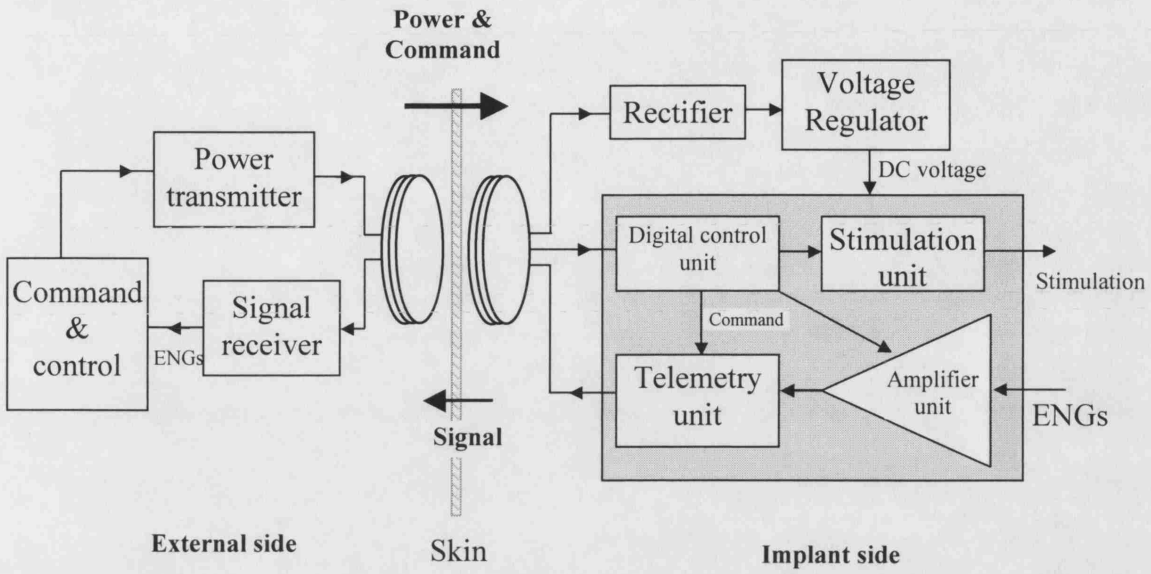


Fig. 1.1 Illustration of a feedback controlled implantable neuroprosthesis.

Closed-loop devices using EMGs and a signal from a joint angle transducer as feedback have been reported in the literature [76, 91], but fully implantable devices controlled by ENG have not been seen. Technologies involved in neuroprosthesis design consist of four fields: RF power and forward signalling, implantable stimulation techniques, neural recording techniques and ENG telemetry. As a result of extensive development in implantable stimulation and neural recording methods, over the past 40-50 years, techniques in RF powering, forward data transmission, electrical stimulators, electrode design and amplifier design are more or less ready to use.

The ENG telemeters, on the other hand, are very rare. In most laboratory experiments on neural recordings, the signals are carried out of the body by transcutaneous wires before amplification and analysis. The open skin wound may cause localised infections and necrosis, requires maintenance, and may not be acceptable to patients due to the poor cosmetic appearance.

In one of a few exceptions, the foot-drop correction experiment mentioned above, the sural nerve signal is conveyed outside the body by a single channel ENG telemetry system [108]. After signal processing, a command is generated to control a separate implant stimulator system to activate the peroneal nerve. Although it is a fully

implantable close-looped system as a whole (Fig. 1.2), such an arrangement may only be feasible for laboratory research because each implanted device requires a separate surgical location and a separate RF power supply.

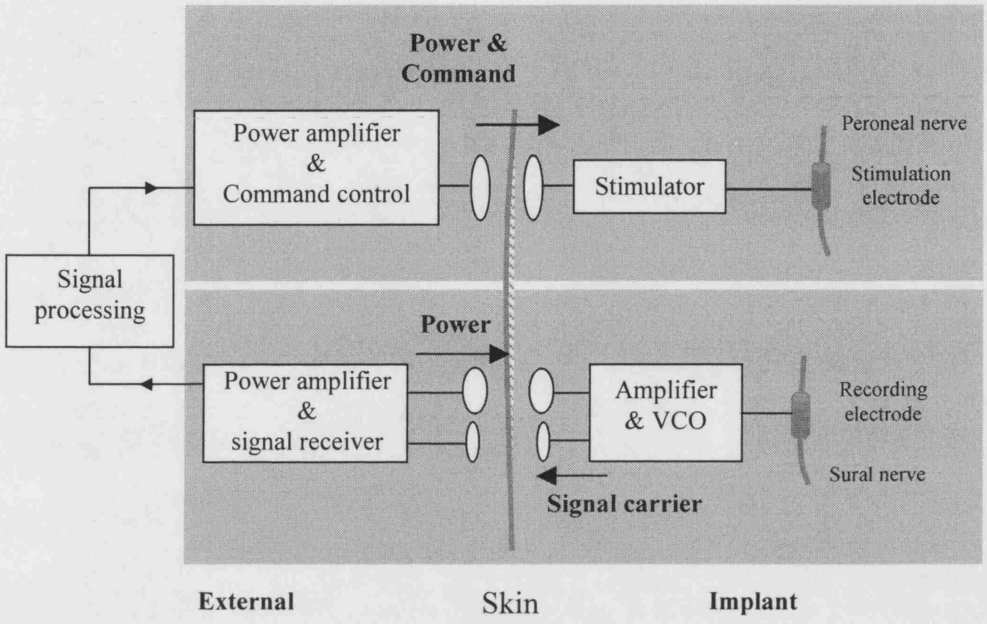


Fig. 1.2 The close-looped system used in the foot drop correction experiment.

Therefore, telemetry methods, which are not only capable of transmitting ENG but also simple to implement in neuroprostheses, need to be explored. This thesis intends to describe the development and investigation of such a method. As a demonstration example and also as part of a project for a closed-loop controlled bladder stimulator being developed at the Department of Medical Physics & Bioengineering, UCL, London, a two channel ENG telemetry system design is presented in the thesis.

1.2 What are the requirements for ENG telemetry in feedback neuroprosthesis?

In general, the telemetry should be easily integrated with the rest of the system; it should not degrade the performance of the other subsystems, and it must be capable of transmitting ENG signals. It mainly requires the following:

Power supply: most of the implantable neuromuscular stimulators are RF powered. Hence, the telemetry system should adopt the same power source.

Working range: the implant unit will be surgically implanted just under the skin and fat tissue. When the device is in use, the external antenna will be placed over the implant outside the body. Thus, the required working distance between the implant and external antennae, for both power channel and signal channel, must be greater than tissue thickness, which for most individuals is between 10 mm - 70 mm.

Design simplicity: for an implantable system, a simple design is much preferred, as it reduces implant size and improves reliability.

Power efficiency: the whole prosthesis will be designed as a portable system to allow the patient to use it continuously for most of the day (more than 12 hours). Therefore, good energy efficiency is essential.

High transmission rate: in order to transmit ENG, a high data transmission rate (or large bandwidth) is needed. In digital transmission, the required minimum transmission rate is determined by

- the number of channels
- the sample rate
- the number of digital bits in the A/D converter
- the coding scheme

The sample rate must exceed twice the maximum frequency in the signal spectrum. The recorded ENG spectrum depends on the shape of the action potentials composing the signal, and also on the electrode geometry and configuration [53]. It usually lies between a few hundred Hz and 10 kHz with maximum power being below 3 kHz [52, 54, 75, 80, 93]. In general, an ENG contains higher frequency components compared to other biological signals. Hence, the sample rate needs to be higher.

The number of digital bits required in the A/D converter is determined by the signal resolution, the signal dynamic range and the noise level. *Resolution* is the smallest amplitude changes that need to be distinguished. *Dynamic range* is the amplitude ratio of the largest signal to the resolution. The noise floor is made up of the thermal noise plus some background nerve activities.

The amplitudes of the nerve signals recorded from intact peripheral nerves are in μV level, varying with axon sizes, number of active axons, cross-sectional area of the nerve and length of the recording nerve cuff [52-54, 93]. For examples, ENG signal amplitudes recorded from mammalian limb nerves during normal movements typically range from about 5μV to 90 μV [52]; ENG elicited from cutaneous receptors or muscle spindles in human applications are typically within 10 μV [46, 47, 49, 87, 89]. Sometimes it is less than 1 μV [49, 52, 60, 61].

Apart from naturally-occurring ENGs, Compound Action Potentials (CAP) are often measured to estimate the nerve conduction velocity, to assess nerve damages during or after a surgical operation, and to check the electrode conditions. A CAP is generated when the axons in a nerve are synchronously activated by a brief electrical stimulus delivered via electrodes. Its amplitude is much larger than those of naturally-occuring ENG, and could be in a range of 10 μV to more than 100μV [53].

The noise generated from the electrodes and the amplifiers, according to other researchers [75] and the author's own experience [30, 108], is around $0.5\mu V_{rms}$-$0.7\mu V_{rms}$ in 8 kHz bandwidth.

Given that the noise and the small ENGs are both at sub-μV level, the resolution for the A/D converter must be better than 0.1 μV in order to distinguish the signal from the noise floor. Given the large amplitude span of the signals and the required resolution, an ENG signal has greater dynamic range compared to other biological signals. It requires more digitised bits in the A/D converter.

Therefore, if the number of channels and the coding scheme are the same, compared to that required for other biological signals, the data transmission rate for ENGs will need to be much faster.

In our project, we need to transmit two ENGs recorded from the bladder-related nerves. Current knowledge on these ENG characteristics is limited. Jezernik et al. [60, 61] observed from experiments performed in anaesthetised pigs and cats that, during bladder contraction, the ENGs from sacral sensory nerve roots increased as little as 0.2 μV above the noise floor. Further research is necessary to characterise the signals in

humans during normal daily activities. However, based on (1) the estimates from the ENGs recorded on other human nerves [49], (2) the size of human sacral nerve roots [56, 84], and (3) the type of nerve fibre (Aδ & C fibres) [25], it would be reasonable to define the amplitude range of the bladder-related ENGs as within –30 μV to 30 μV, the required resolution as 0.1 μV, and the bandwidth as less than 5 kHz. Therefore, a 10 bit A/D converter is sufficient to cover the dynamic range ((30-(-30))/0.1= 600), and the sample rate must be at least twice of 5 kHz, becoming 10 kHz. If each sample is coded with 1 additional bit for error check and word synchronisation (to be discussed in Chapter 7 and 8), the required bit rate for transfering two ENGs will be

no. of channels × sample rate × (no. of bits in A/D converter + parity bit),

that is

2×10 kHz×(10+1) bit = 220 kHz

To summarise, it is prefered that an ENG telemeter in a feedback neuroprosthesis design has following properties:

- High data rate
- Simple design
- RF powered
- Low power consumption
- Sufficient working distance
- Does not degrade or interfere with the performance of other parts of the system, such as power transfer and ENG amplification.

Preferably, all these objectives should be achieved simultaneously. *Would an existing method in the telemetry field be found to satisfy these requirements?*

1.3 Data transmission in biotelemetry

1.3.1 Introduction

Signals can be transmitted wirelessly via acoustic waves, radio, or light. Radio transmission is most commonly used. Although sharing some common methodologies

with radio engineering, biotelemetry has its own ground in many aspects. Its design is compelled by demands for miniaturisation, low power consumption, and simple circuitry. It is mainly made up of two components: the control unit and the remote unit (Fig. 1.3). The remote unit is located on the object whose parameters are to be measured. The communications between the two units via antenna allow measured data and control commands to be exchanged. In some applications, energy transfer is also involved.

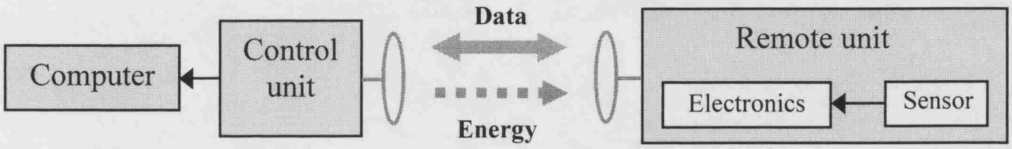


Fig. 1.3 Diagram of a telemetry system

The transmission range is not clear-cut. Usually long-range telemetry can cross hundreds of meters or even much longer distance; medium-range works in the region of 10 cm to a few meters; close-range telemetry typically couples between 0 to 10 cm.

Transmission formats are diverse due to various design possibilities and requirements of the applications. There were reviews of the technology prior to 1980 [2, 66, 68, 106], and also of some particular types of device [83, 95, 102]. Since the 1980s, new methods and devices have emerged, but no clear agreement has been reached on the classification of currently available telemetry transmission methods. In the author's opinion, they fall into two categories: active transmission and passive transmission, respectively illustrated in Fig. 1.4 and Fig. 1.5. In active transmission, the remote unit comprises a local oscillator, radiating an RF carrying data information collected from the object (Fig. 1.4). In passive transmission, the remote unit does not contain a local oscillator. It is the control unit which radiates the RF carrier. The remote unit sends the signals by responding to this incoming RF (Fig. 1.5). Within each category, Amplitude Modulation (AM), Frequency Modulation (FM), Phase Modulation (PM) and mixed modulation are all possible.

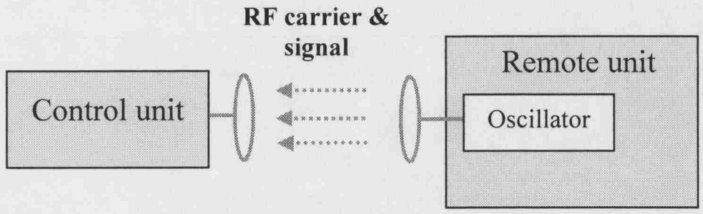


Fig. 1.4 Active telemetry

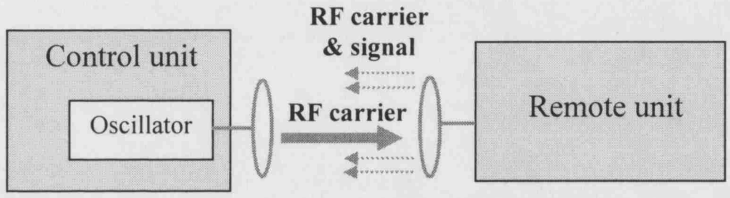


Fig. 1.5 Passive telemetry

1.3.2 Active transmission

Active transmission has been summarised by Ko [66], Mackay [68], and Jeutter [58]. A steady unchanging RF emission would allow the control unit to determine the object location. A modulated RF can carry more sophisticated information. Because the object (animal or human) often moves, frequency or phase modulation is usually chosen to overcome motion artefact. For example, a blocking oscillator's on and off rate (blocking rate) can indicate the temperature or the pressure [66, 68]. Direct continuous FM or PM for transmitting electrical signals (ECG, EMG, ENG, etc) can be made by modulating a single transistor RF oscillator such as Colpitts or Hartley circuits [35, 58, 66, 68, 83], by an off-the-shelf voltage to frequency converter [71, 108], or by a custom designed integrated circuit (IC). A power amplifier is sometimes added to enhance the transmission range [32]. The active transmission is suitable for applications covering all working-ranges. Medium and long-range telemeters almost exclusively use active transmission.

1.3.3 Passive transmission

There are three underlying operational principles of passive transmission in biotelemetry[2]: inductive coupling, (sub) harmonic re-radiation and backscatter reflection.

1) Inductive coupling

At close range, the antennae of the remote unit and control unit, usually a pair of looped coils, form an inductive coupling circuit. The circuit parameters of the remote unit directly affect the current in the antenna of the control unit.

The simplest example is the grid dip meter approach for pressure measurement inside a body [68]. The remote unit is in the intracranial, bladder or gastrointestinal location. It incorporates a capacitor, a coil and a ferrite core. Its resonant frequency varies as the pressure changes move the ferrite core in or out of the coil. Outside the body, a 'grid dip meter' emits radio waves in a range of frequencies, which reach the implant through the skin. The grid current is monitored. If a scanning frequency meets that of the implant, a *dip* will be noted. From the pre-calibrated pressure-frequency relations, the corresponding pressure is then known.

In the 1980s, several researchers developed a passive method for digital binary data transmission. It is called *Passive Impedance Modulation*, based on the principle of impedance transformation by two inductively-coupled coils (Fig. 1.6).

[2] Passive transmission is also a dominant procedure adopted by Radio Frequency Identification (RFID) tags, in which the remote unit does not contain a sensor, but rather has the data pre-stored. Currently, RFID is gaining popularity in commercial applications of contactless smart cards, fare systems for public transport, access control, container identification, goods transport and industrial automation. For reference in the RFID field, See Finkenzeller [33] .

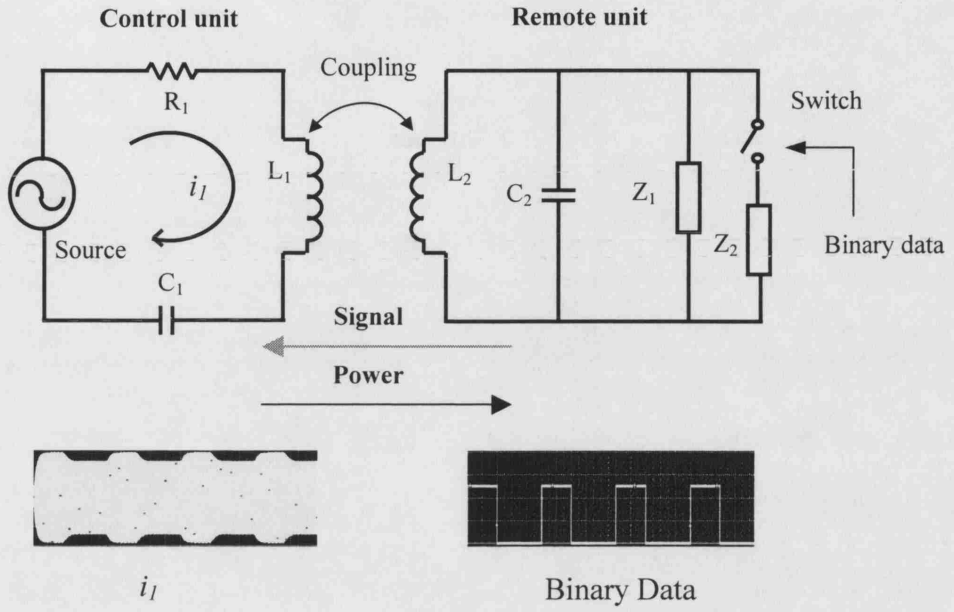


Fig. 1.6 Illustration of passive impedance modulation

In Fig. 1.6, L_1 and L_2 represent the antennas, which are usually inductive. The L_1C_1 circuit in the control unit and the L_2C_2 circuit in the remote unit are both tuned to resonance at the transmission frequency. When the antenna coil L_2 approaches L_1, the influence of the remote unit on the control circuit is equivalent to an additional load. If a stream of binary data turns the switch on and off, the load will vary correspondingly. The change is reflected in the L_1 current when the L_1C_1 circuit radiates RF for transmitting energy into the remote unit. Therefore, the energy passes inwards to the implant and the signals pass outwards through the same pair of coils at a common carrier frequency.

Passive Impendance Modulation can send digital information, and has simple circuit configurations. The applications include EMG and ECG monitoring [99], EMG and pressure monitoring in the uterus of cows [74], and disease detection and management of livestock [67]. Most RFID systems are in fact of the impedance modulation type [33].

2) (Sub) harmonic re-radiation

In this method, the control unit radiates a RF with a defined frequency f_G, usually for power supply. At the remote side, apart from being converted to a DC voltage, the f_G is factored down to a subharmonic f_G/N (while N is 2, 3, 4 etc.). f_G/N then acts as a data carrier, and is modulated by the binary data stream. The modulated f_G/N is fed back into the remote unit's antenna directly, or via an output driver, sending data back to the control unit.

DeMichele and Troyk have achieved a high data rate by phase modulating the subharmonic $f_G/2$ (one bit every 16 cycles of the RF carrier). However, at the control unit side, amid the high intensity of the magnetic field at the frequency f_G, detection of the weak signal carrier $f_G/2$ is not easy. DeMichele and Troyk designed a unique magnetic structure to detect the $f_G/2$, but it is also quite complicated [26]. Another disadvantage, indicated by Finkenzeller [33], is that this procedure often operates in the long wave range at 100-135.5 kHz. For example, f_G in DeMichele and Troyk's system is 134 kHz.

3) Backscatter reflection

In this approach, the underlying principle is similar to that in RADAR (Radio Detecting and Ranging) technology. When an electromagnetic wave emitted into the surrounding space encounters an object with dimensions greater than around half the wavelength, part of its energy is absorbed, and part of it is reflected by the object back to the space. The antenna in the control unit intercepts a small portion of scattered wave. The amount of reflection depends on the property of the object. When its dimension is comparable to the wavelength, for example a ½ wavelength dipole antenna, the reflection is strong. If the antenna reflection property is modulated by a binary data stream, the control unit will detect the corresponding magnitude variation in the scattered wave [33]. The method often works at microwave frequency (GHz) due to the possibility in this frequency region of using small antennas, whose sizes are comparable to the wavelength. See Table 1.1.

Table 1.1 Frequency and wavelength relation

Frequency f (Hz)	10k	100k	1M	10M	100M	1G
Wavelength λ (m) (by $\lambda = c / f$, $c \approx 300\,000$ km/s)	30000	3000	300	30	3	0.3

1.3.4 Multi-channel transmission

In case several physiological signals are required simultaneously, they are conditioned by either frequency division multiplex or time division multiplex to form a composite signal that could be sent via the radio links described above. There are some implemented examples in the literature [31, 35, 58, 66, 68]. For multi-device or multi-patient management, modern multiplexing techniques such as spread spectrum and frequency hopping provide efficient use of the available radio spectrum, reliable communication, and possibly a readily available system for biomedical applications [4, 83].

1.3.5 Power supply and frequency choice

Powering the remote unit is usually by two means: built-in batteries or RF powering, although there are a few other possibilities [68]. Batteries can be used in applications of any range; RF powering is mainly suitable for short-range devices. Although there were a few RF powered systems working in medium range, the required power output from the control unit was rather large [35, 65]. For long-term implantable applications, RF powering is preferred because it allows the implanted devices to be totally inert and be placed in the patient's body without side effects throughout his life time. Many implanted FES neuroprotheses are RF powered, and they work in close-range. An additional benefit of using RF powering is that the link can be utilised for signalling. Both passive impedance modulation and sub (harmonic) reradiation transmission have this advantage.

The telemeter operating frequency chosen by the researchers covers 50 kHz to a few hundred MHz [68], or even higher [83]. The selection of the frequencies is

influenced by many factors, see Appendix 1. In the case of the implantable device, the choice of the frequency is a compromise between two requirements: to keep the tissue absorption low and to make the implant size small. In the case of the frequency of the power carrier, the performance of the power amplifier under various frequencies also needs to be taken into account [28]. Therefore, the frequency of implantable neuroprothesis power carrier is often in the range 1~ 10 MHz [1, 28, 101, 109], and a few work between 10 MHz ~ 20 MHz [37, 51].

1.3.6 Summary

The data transmission methods discussed above are summarised in Fig. 1.7. Data transmission in biotelemetry has two divisions: active transmission and passive transmission. Each division consists of several sub-methods. Active transmission is mostly used because it is suitable for wider ranges of application, has more choices of power supply and of operating frequency; and sometimes the technology and commercial components from telecommunication field are readily adapted. But its circuitry is relatively complicated. Although passive transmission is limited for applications in close-range and medium-range, its circuit design is much simpler. For a close-range and RF powered system like a neuroprosthesis, both transmission approaches can be applied, and in some situations passive method is preferred (see next section).

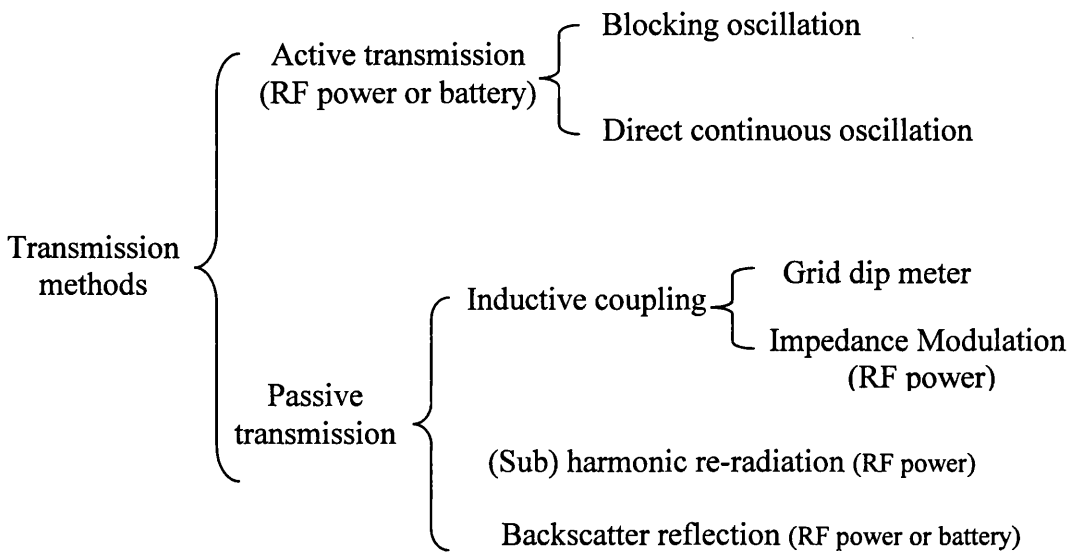


Fig. 1.7 Summary of signal transmission methods

1.4 Limitations of existing methods.

Most biotelemeters were designed for conveying low frequency biological signals, like temperature, pressure, ECG, or EMG, etc. Little has been published on ENG telemetry design at the time of writing this thesis. Zhou et.al [108] developed a single channel ENG telemetry system using an active transmission approach. A voltage-controlled oscillator is in the implant, it radiates a frequency modulated carrier at 380 kHz, and sends a neural signal to the external side. Several such devices have been implanted in human and animals since 1999 in laboratory studies. One of them is for foot drop correction, the research mentioned in section 1.1. Fig. 1.8 shows the telemeter system and Fig. 1.9 shows an ENG recording by this device.

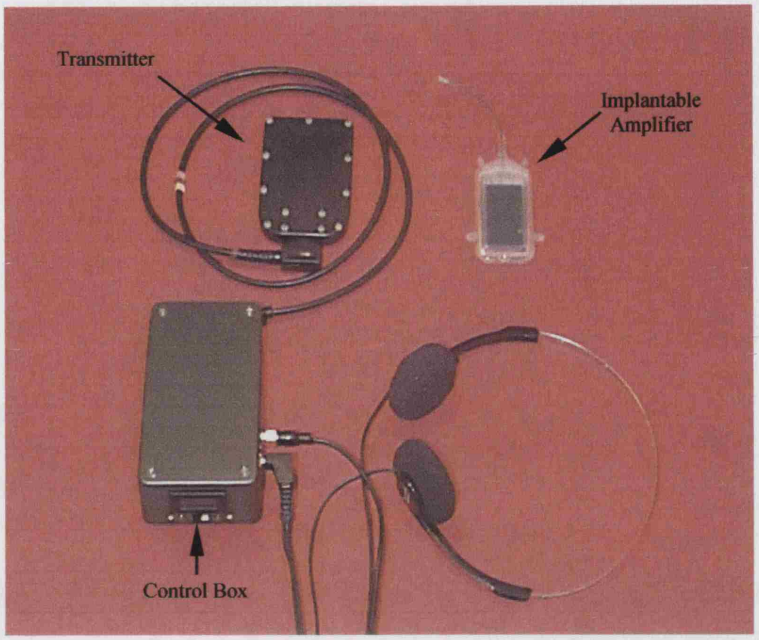


Fig. 1.8 The single channel ENG telemeter system (the photo is taken by the author).

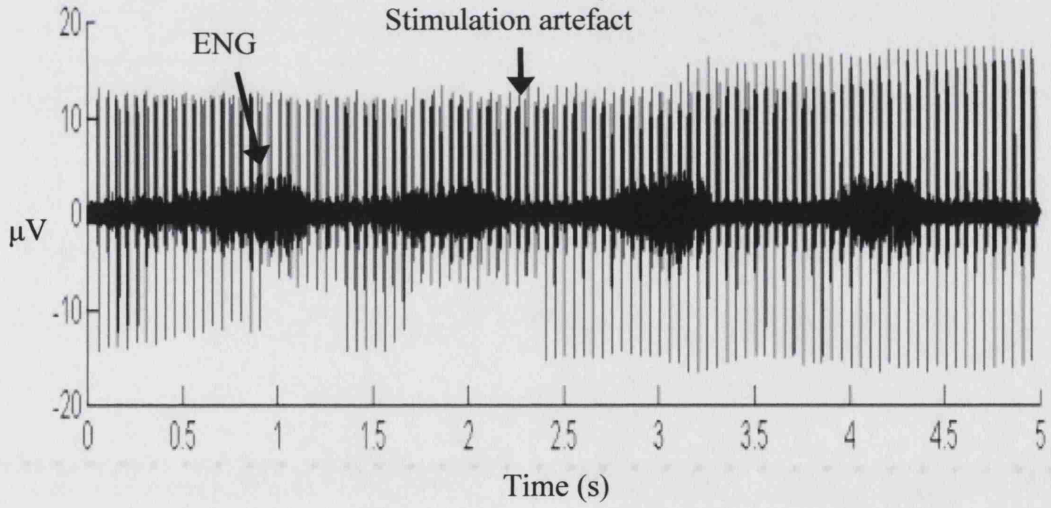


Fig. 1.9 ENG recorded on the Volar digital nerve from a tetraplegic spinal cord injured patient, taken while a stimulator caused the hand to close and the experimenter stroked the index finger (Unpublished, courtesy of SMI, Aalborg University, Denmark).

Although it has been proved a feasible method [29], for ENG transmission, like most neuroprotheses, it is powered by radio frequency. An RF at 4 MHz is transmitted inwards to supply energy to the implant. Therefore, some design problems need to be

considered. First, two pairs of antennae have to be used: one is for the power channel; the other is for the signal (Fig. 1.10). Second, the antennae need to be carefully designed in order to reduce cross talk between the two channels [27]. Third, the frequencies of the power and signal carriers should be well separated to avoid cross channel interference, and to let the power carrier being adequately attenuated by the filter in order to detect the weak signal carrier at the external side. Finally, experiences gained from this design show that it is not easy to predict the effect of RF interference from both channels on the implant ENG amplifier, which has a large gain. In some circumstances, it might increase the noise level, and in others the interference could be so severe that it stops the amplifier's operation.

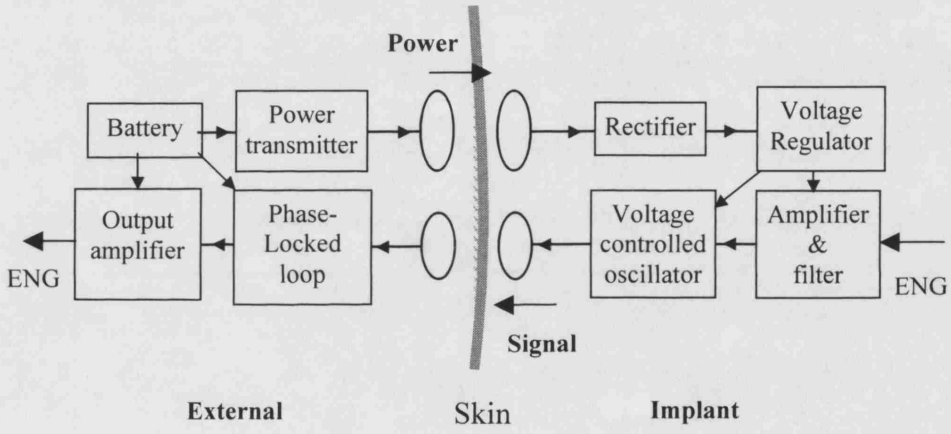


Fig. 1.10 Diagram of the single channel ENG telemeter.

The most undesirable feature of active methods is the two pair antennae arrangement. They add circuit complexity and occupy precious space at the implant side. For an implant telemeter, such complexity might be acceptable. However to integrate with an already complicated stimulation system, a simpler method is much more desirable.

The two pair antennae problem exists if the backscatter reflection method is adopted, as the signal carrier would work at microwave frequencies, while the power carrier would not exceed 20 MHz. As for the grid dip meter and sub (harmonic) re-radiation approaches, both of them require complicated detection circuits at the external side.

Passive impedance modulation is very attractive as it has a much simpler structure. It uses the same pair of antennae, on a common carrier frequency, to pass the energy to the implant and transfer the signals outwards. The Cleveland group used it in a EMG feedback controlled hand-function stimulator [96]. In many RFID systems, this method is also chosen for its simplicity [33].

However, the major obstacle to utilising it in ENG transmission is that its data rate is not high enough. A higher data rate might be achievable by manipulating the circuit parameters, for example reducing switch closing time, but working range or energy efficiency have to be sacrificed. The Michigan group reported a custom designed integrated circuit adapting this method for wireless recording neural signals from a micromachined sieve electrode [1], but the working distance ($k \approx 0.082$ or 5mm ±20%) is inadequate for a human worn implant. Increasing the carrier frequency also allows higher data rate, but the carrier frequency cannot go up indefinitely due to loss of power efficiency by increased tissue absorption.

In conclusion, there is no transmission method which satisfies all the requirements set up in Section 1.2. The active transmission and some of the passive methods do not satisfy the simplicity requirement, while in passive impedance modulation, the speed and working distance can not be achieved simultaneously. Exploring new possibilities is necessary. Using one pair of antenna for both power and signal transmission, as in impedance modulation, has the obvious advantage of simplifying the circuit. This is a feature worth keeping.

1.5 Thesis objectives

The aim of this thesis is to develop a new passive modulation method, which achieves the following objectives:

- keeps the simplicity as in impedance modulation by using the single pair antennae arrangement for both power and data transmission,
- achieves high data rate without necessarily increasing carrier frequency,
- works up to a sufficient distance,

- without degrading power transfer performance.

The method is termed by the author *Passive Phase Shift Modulation* (PPSM). Prior to the thesis, the preliminary results have been presented in [107]. The scheme transmits phase shift modulation from the implant, but results in amplitude modulation in the external side. It should provide a simple but effective approach to conveying ENG signals from within the body at a high bit rate/carrier frequency ratio for neuroprostheses design. PPSM might also find broader applications in the RFID industry. In this field, most products use impedance modulation for signalling. High-speed options are being more intensively searched in order to improve the reading speed which will no doubt contribute to increased productivity.

1.6 Thesis structures and hypotheses

The thesis is arranged in 4 parts consisting of ten chapters:

1. *Part 1 Introduction*, including
    - Chapter 1 introduction and objectives
2. *Part 2 Theoretical analysis*, including
    - Chapter 2 Inductive link for RF powering
    - Chapter 3 Introducing *Passive Phase Shift Modulation*
    - Chapter 4 Analysis of *Passive Phase Shift Modulation* – part 1
    - Chapter 5 Analysis of *Passive Phase Shift Modulation* – part 2
3. *Part 3 System design*, including
    - Chapter 6 PPSM system design – overview and the transmitter circuit
    - Chapter 7 PPSM system design – the implant circuit
    - Chapter 8 PPSM system design – the external circuit

- Chapter 9 PPSM system design – assessment and test

4. *Part 4 Discussion*, including

    - Chapter 10 Discussion

These chapters discuss the research and development on following order:

1. Introducing and analysing RF power transmission by an inductive link.
2. Introducing the principle of PPSM; comparing PPSM with conventional *Impedance Modulation.*
3. Analysing the transient response of the coupled circuit. Deriving the mathematical function of the PPSM waveform.
4. Interpreting the analytical results and analysing how the modulation is affected by the circuit parameters.
5. Designing the electronic system to realise PPSM.

The following hypotheses will be tested in the thesis:

1. PPSM has advantages in speed, working range and energy efficiency compared with conventional *Passive Impedance Modulation.*
2. The power loss in PPSM is mainly due to resistance in the primary circuit.
3. The transient waveform generated by PPSM is in good shape for demodulation within the required working range.
4. The switch closing action only changes the i_2 phase, and will not affect any other currents and voltages.
5. The circuit parameters, optimised for power transfer efficiency, are also good for signalling.

Part 2

Theoretical analysis

Chapter 2 Inductive Link For RF Powering

2.1 Introduction

The inductively coupled RF link for energy transmission is one onto which the passive data transmission will be superimposed. Its circuit configuration and typical component values are also featured in the passive data link. This chapter describes the design of an optimised RF link which will be used throughout this thesis. The optimisation emphasises maximising energy efficiency and is done by choosing proper coils (antennae).

In the following sections, the literature is reviewed; the prior knowledge used in the design and the author's contribution are stated; circuit configuration is described and the RF power link analysed; and the design procedure is demonstrated in an example. Finally, signal phases in the coupled circuits are explained.

2.2 Background

There are many aspects to consider when designing an RF link for an implant neuroprosthesis: size and location of the implant, power and regulation requirements, package property, communication bandwidth, complexity of the receiver and transmitter circuits, power supply, misalignment and displacement tolerance, efficiency, etc. [101]. The link properties related to implant design have been studied in several aspects. Flack et al. [34] calculated the mutual inductance of air-cored coils. Geselowitz et. al. [38] investigated the effects of metals on transcutaneous energy transmission. Soma et. al. [92] presented theoretical misalignment analysis of coupled coils. Heetderks [50] examined the feasibility of RF powering of millimetre- and submillimeter-sized "Microimplants". Terman [97] and Grover [42] provided engineers with the handbooks for general inductive circuit design.

Inductive coupling is often realised by a pair of circular coils made of a few turns of solid copper wires[1]. One coil lies beneath the subcutaneous tissue and the other is positioned over it on the skin surface. As conventions, the transmitter or primary coil

[1] Or Litz wire, which is multi-stranded copper wire.

refers to the coil at the external side, and the receiver coil or secondary is the one at the implant side.

In a practical situation, the coils are substantially separated by thick tissue (for example, in the abdomen or thigh), so the coupling between them is weak and the RF power transfer is lossy.

Also in the practical situation, when one breathes or is active, the under-skin tissue moves causing changes in coil alignment and coil distance. Tissue thickness varies from person to person too, giving differences of coil separation among individuals. The changing alignment and separation result in a variable coupling between the coils. It will have two consequences: firstly, the circuit optimised for high efficiency in one position might not perform well once the coil moves to another position. Secondly, the voltage obtained in the implant may vary substantially. If output of the implant coil is regulated to maintain a stable DC supply, this could result in the voltage drop across the regulator being too large in some coupling, and insufficient in another. The large drop wastes energy, and the insufficient drop makes the regulator's output level unsustainable.

Therefore achieving high efficiency and good displacement tolerance are the main focuses of the RF power link design.

One approach to maintain a better displacement tolerance is to reduce the variation in coupling. Using an external coil larger than the implant coil can partly serve such a purpose [33, 34, 51]. With this arrangement, the coupling coefficient remains fairly constant when the small coil moves laterally around the larger coil, as long as within the larger coil's perimeter. It is, however, still sensitive to coil separation, and if the external coil is substantially oversized compared to the implant coil, the coupling when two coils are close will be sacrificed, which consequently reduces efficiency. Therefore, it does not have any obvious advantage in auditory prosthesis design. Even in those applications that work at greater coil-coil distance, for which a larger coil will give not only less variable but also a possibly higher coupling coefficient at the desired distance, the size of the external coil still has to be limited because it would be too impractical for a patient to carry if it were too large [28].

To improve displacement tolerance, apart from manipulating the coil size, the most common approach is through the design of the coupled transmitting and receiving circuits. Galbraith et al [37] employed stagger tuning. In their method, both transmitter and receiver are tuned off the operating frequency, one below and one above. If the resonant frequencies are chosen properly, when the coupling changes they shift in a manner that compensates the gain at the fixed operating frequency. Zierhofer & Hochmair [109], on the other hand, let the operating frequency track the coupling variation to obtain stable gain and efficiency. Donaldson & Perkins, Forster, and Hochmair [28, 36, 51] exploited the feature of the secondary voltage being least sensitive to coupling change if it is near maximum. Because the maximum occurs at the critical coupling, their effort was on arranging the link parameters so as to work close to this critical value.

Enhancing coupling coefficient can improve efficiency. Galbraith et al. [37] recommended using ferrite backing. Zierhofer & Hochmair [110] suggested winding the coils in a way that distributes the turns across the radii instead of concentrating them at the outer circumferences. Ko et al [64] have shown that if the receiver coil diameter is known, there exists an optimal transmitter coil diameter that will maximize the coupling at a given separation. Another approach for improving efficiency is by properly choosing the component values of coupled circuits. Donaldson & Perkins [28] showed that there is an optimal number of turns for the coils.

Although there are several studies on RF link design in the literature, most approaches apply to situations of high working value in coupling, such as for cochlear neuroprostheses [37, 109]. The link which Donaldson & Perkins [28] studied resembles the situation studied by this thesis. Therefore, their design approach is considered. However, several modifications and improvements are made here: firstly, on circuit tuning. Donaldson & Perkins's design tuned the primary circuit to the operating frequency and the secondary to a slightly higher frequency, which makes the secondary impedance appearing in the transmitter circuit real at all coupling. With such an arrangement, simple formulae were derived and the transmitter tuning was not altered by the presence of the receiver. Practically, however, this approach makes frequency adjustment complicated. For every modification of the implant coil and the load in

particular, the transmitter operating frequency has to be readjusted. If the transmitter frequency is set by a crystal oscillator, such a change will not be convenient. Therefore, in the author's design, both coils are tuned to the same resonant frequency, and the formulae for such tuning are derived accordingly. Secondly, using quality factor Q rather than discreet L, R and C describing an inductive circuit helps simplify the analysis and gives a better understanding of the problem. This advantage is accordingly demonstrated in this chapter to help reduce iterative procedures when selecting primary coils. So, in this thesis, following other researchers [64], Q is used whenever it is suitable. Thirdly, in both examples given in their paper, Donaldson & Perkins focused on achieving the design goals at a specific coil spacing. However, normally the performance over a range of coupling rather than one single position is much more concerned. Hence, a graphic approach which plots the efficiency versus coupling and the voltage gain versus coupling is added to assist evaluating the overall performance of the circuit parameters. Fourthly, from the author's experiences it is found that for cases in which the coupling coefficient is in the middle range, say 0.01 ~ 0.16, optimal efficiency and optimal displacement tolerance partly overlap. Therefore, the design can always start from the maximising efficiency point of view and it usually results in good displacement tolerance as well. Finally, the proper selection of coil geometric size could result in a higher coupling, which would contribute to higher power transfer efficiency. Combining this with the selection of optimal numbers of coil turns will give a better result. This has not been emphasised by Donaldson & Perkins [28] as they considered the coil size mainly from the displacement tolerance point of view.

The following sections will explain the design approach in detail.

2.3 Circuit configuration

Either the primary or the secondary circuit could be series or shunt-tuned, giving four possible combinations [37]. The configuration in which the primary is series-tuned, with the secondary shunt-tuned, has an input-output property of voltage in-voltage out, which is convenient for connecting a class D transmitter (a voltage source) at the input and a voltage regulator at the output.

The link circuit is shown in Fig. 2.1. The primary resonant frequency is tuned by the primary coil L_1 and the capacitor C_1, and in the secondary is by L_2 and C_2. The voltage source, v_s, represents the transmitter output signal. R_0 is the transmitter output resistance. R_t is the series loss resistance in L_1. R_r is the parallel loss resistance in L_2. R_L represents the implant electronics. D is a rectifying diode and C_3 is a large smoothing capacitor. Note in the secondary circuit a half-wave rectifier is used rather than a full-wave rectifier. Given a similar AC to DC conversion efficiency, the half-wave rectifier has simple circuit, and the DC voltage only drops one diode-forward-voltage from the AC peak voltage. Although larger ripples result after rectification, they can be smoothed out by a large capacitor C_3.

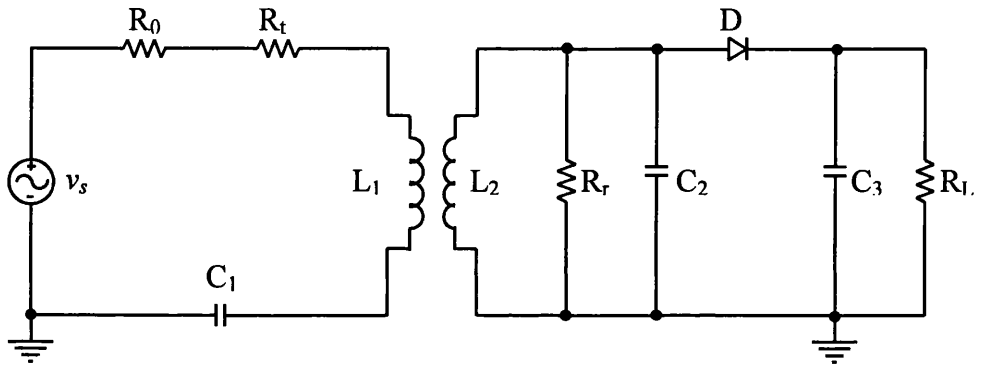


Fig. 2.1 Inductively coupled circuit for power transmission.

For analysis convenience, an equivalent load R_{eq} is used to summarise D, C_3 and R_L (see Fig. 2.2).

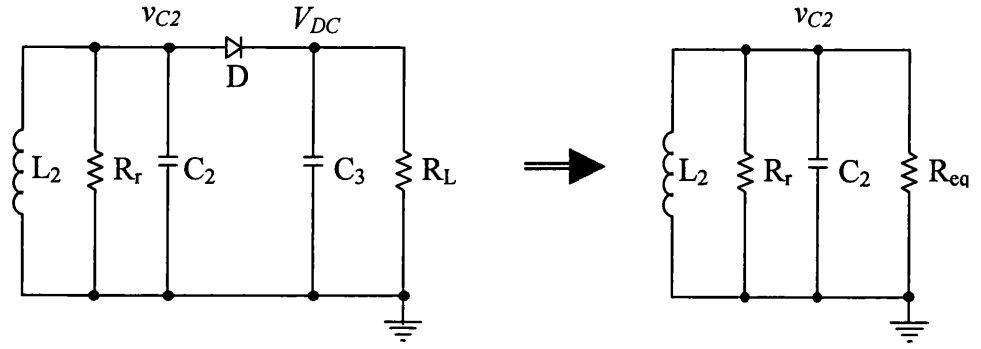


Fig. 2.2 The secondary circuit with DC load and the equivalent circuit with AC load.

The derivation of their relationship is as following [64]:

In the left diagram of Fig. 2.2, neglecting the voltage drop across D and the voltage fluctuation on C_3, the power dissipated in R_L is

$$P_1 = \frac{V_{DC}^2}{R_L} = \frac{V_{C2}^2}{R_L} \quad \text{------ Eq. 2.1}$$

In which V_{C2} is the magnitude of v_{C2}. V_{DC} is the DC voltage on R_L. In the right of Fig. 2.2, the power dissipated in R_{eq} is

$$P_2 = \frac{V_{C2rms}^2}{R_{eq}} = \frac{1}{2}\frac{V_{C2}^2}{R_{eq}} \quad \text{------ Eq. 2.2}$$

Where V_{C2rms} is the root-mean-square value of v_{C2}. If the two circuits in Fig. 2.2 are to be equivalent, the dissipated power must be equal, that is

$P_1 = P_2$, therefore

$R_{eq} = ½ R_L$ ------ Eq. 2.3

If

$R_1 = R_t + R_0$ ------ Eq. 2.4

$R_2 = R_r // R_{eq}$ ------ Eq. 2.5

Fig. 2.1can be simplified as shown in Fig. 2.3. This circuit configuration will be used throughout this thesis, with the signals and sign conventions marked in the diagram.

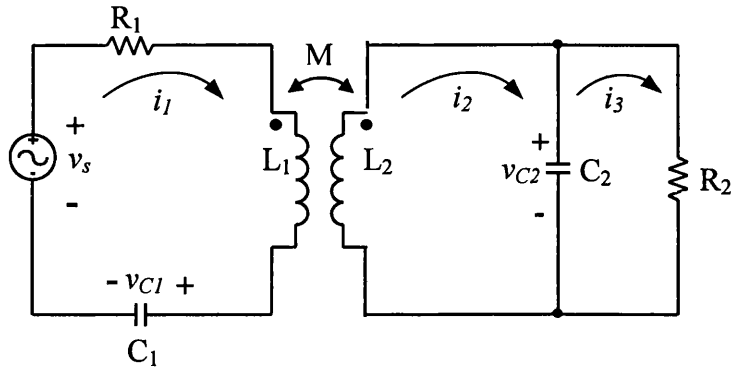


Fig. 2.3 Inductively coupled circuit for power transmission in the analytical form.

2.4 Circuit responses

The voltage source is approximated by a sinusoidal waveform having angular frequency Ω, magnitude E, as

$$v_s = E\cos(\Omega t) \qquad \text{------ Eq. 2.6}$$

From the components and connection constraints shown in Fig. 2.3, the KVL (Kirchoff's voltage law) equation in the phasor domain for steady-state response can be written as: (See Appendix 2 for the rules of voltage and current reference assignments for a pair of coupled coils)

$$\left.\begin{aligned} &(R_1 + j\Omega L_1 + \frac{1}{j\Omega C_1})\, I_1 - j\,\Omega M\, I_2 = E \\ &-j\Omega M\, I_1 + j\Omega L_2\, I_2 + \frac{1}{j\Omega C_2}\,(I_2 - I_3) = 0 \\ &\frac{1}{j\Omega C_2}(I_3 - I_2) + R_2\, I_3 = 0 \end{aligned}\right\} \qquad \text{------ Eq. 2.7}$$

Where I_1, I_2, and I_3 are phasor currents, M is mutual inductance, and the primary and secondary are both tuned to the operating frequency Ω, there is

$$\Omega^2 = \frac{1}{L_1 C_1} = \frac{1}{L_2 C_2} \qquad \text{------ Eq. 2.8}$$

Let Q_1 and Q_2 be quality factors of the primary and secondary circuits, k is the coupling coefficient. By definition,

$$Q_1 = \frac{\Omega L_1}{R_1}, \qquad Q_2 = R_2 C_2 \Omega \qquad \text{------ Eq. 2.9}$$

$$k = \frac{M}{\sqrt{L_1 L_2}} \qquad \text{------ Eq. 2.10}$$

Solving Eq. 2.7 obtains the magnitudes and phases of i_1, v_{C1}, i_2 and v_{C2} when referring to v_s:

$$I_{1max} = |I_1| = \frac{C_1 Q_1 \Omega}{\sqrt{(1 + k^2 Q_1 Q_2)^2 + k^4 Q_1^2}} E \qquad \text{------ Eq. 2.11}$$

$$\angle I_1 = Arc\tan\left(\frac{1}{\frac{1}{k^2 Q_1} + Q_2}\right) \qquad \text{------ Eq. 2.12}$$

$$V_{C1max} = |V_{C1}| = \frac{1}{\Omega C_1}|I_1| \qquad \text{------ Eq. 2.13}$$

$$\angle V_{C1} = \angle I_1 - \frac{\pi}{2} \qquad \text{------ Eq. 2.14}$$

$$I_{2max} = |I_2| = \frac{\sqrt{C_1 C_2}\, k Q_1 \Omega \sqrt{1 + Q_2^2}}{\sqrt{(1 + k^2 Q_1 Q_2)^2 + k^4 Q_1^2}} E \qquad \text{------ Eq. 2.15}$$

$$\angle I_2 = \angle I_1 + Arc\tan(Q_2) \qquad \text{------ Eq. 2.16}$$

$$V_{C2max} = |V_{C2}| = \frac{\sqrt{C_1 C_2}\, k Q_1 R_2 \Omega}{\sqrt{(1+k^2 Q_1 Q_2)^2 + k^4 Q_1^2}} E \quad \text{------ Eq. 2.17}$$

$$\angle V_{C2} = \angle I_1 \quad \text{------ Eq. 2.18}$$

2.5 Optimising the inductive link

2.5.1 Choosing the coil size and evaluating the working *k* range

The degree of coupling is usually described by coefficient *k*, which is the ratio of mutual inductance actually present to the maximal possible value that can occur. It summarises all geometric factors affecting the mutual inductance so that the coil shapes, separation, colateral and angular misalignment are all concluded in *k* (whose maximal value is 1).

Higher *k* means greater coupling. So, the first design step is to select the coil sizes which will produce the highest *k* at typical working distances. Practically, the selection of the receiver coil is limited by the implant size, so the largest acceptable diameter 45 mm is chosen. If we assume typical coil separation is around 30 mm, following Ko et al [64], a transmitter coil which will maximize coupling at this distance is given by $d_t^2 = 4z^2 + d_r^2$, in which d_t and d_r are the diameters of transmitter and receiver coils respectively, and z is the separation. Thus d_t = 75 mm is obtained. However, it is considered too large for a patient to carry, so 60 mm is used instead.

Having the coil sizes chosen, the *k* values corresponding to coil separations can be found. They can be calculated [34, 42, 92, 97]. But in practice a simple measurement is quicker, see appendix 3. Fig. 2.4 is the measured relation of *k* versus coil spacing. It shows, for a separation of 16 ~ 80 mm, the range of *k* is from 0.16 down to around 0.01.

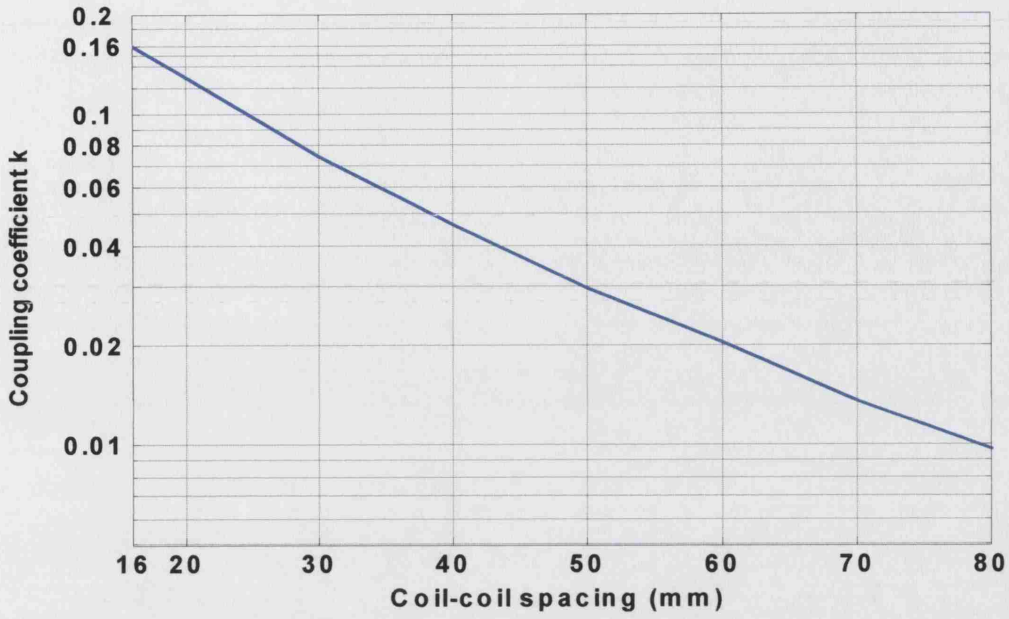


Fig. 2.4 Diagram of coupling coefficient k versus the coil spacing.

2.5.2 Formulae of efficiency and voltage gain

1) **Efficiency**

Referring to Fig. 2.3, the coupling efficiency is defined as

$$\eta_{link} = \frac{power\ dissipated\ in\ R_2}{Power\ from\ voltage\ source\ v_s} \qquad \text{-------Eq. 2.19}$$

In which

$$power\ dissipated\ in\ R_2 = \frac{1}{2} V_{C2}^2 R_2$$

$$Power\ from\ voltage\ source = \frac{\int_0^T v_s(t)\, i_1(t)\, dt}{T_0}$$

Where T_0 is a period of one cycle, $T_0 = \frac{2\pi}{\Omega}$

Substituting Eq. 2.6, Eq. 2.11, Eq. 2.12 and Eq. 2.17 into Eq. 2.19, the coupling efficiency can be represented by k, Q_1 and Q_2:

$$\eta_{link} = \frac{1}{1+\frac{1}{k^2 Q_1 Q_2}} \qquad \text{------Eq. 2.20}$$

Within the receiver circuit, the power dissipated in R_2 is actually shared by R_{eq} and R_r (see Eq. 2.5). Only that in R_{eq} is used by implant electronics (the loss in the diode is neglected). That into R_r dissipates as heat. Hence, the receiver efficiency is

$$\eta_{receiver} = \frac{1}{1+\frac{R_{eq}}{R_r}} \qquad \text{------Eq. 2.21}$$

Multiplying Eq. 2.20 and Eq. 2.21, the overall link efficiency is

$$\eta_{overall} = \frac{1}{1+\frac{1}{k^2 Q_1 Q_2}} \times \frac{1}{1+\frac{R_{eq}}{R_r}} \qquad \text{------Eq. 2.22}$$

2) **Voltage gain**

The voltage gain A is the ratio of the magnitude of v_{C2} to the magnitude of v_s. From Eq. 2.17, or taken from Galbrath's result [37], it is

$$\text{A}=\frac{V_{C2}}{E} = \frac{\sqrt{\frac{L_2}{L_1}}\, k Q_1 Q_2}{\sqrt{(1+k^2 Q_1 Q_2)^2 + k^4 Q_1^2}}. \qquad \text{------Eq. 2.23}$$

It has a maximum A_{max} at critical coupling k_{crit} given by Galbrath [37],

$$k_{crit} = \frac{1}{\sqrt{Q_1 Q_2}\left(1+\frac{1}{Q_2^2}\right)^{1/4}}$$

if $Q_2 >> 1$

$$k_{crit} \approx \frac{1}{\sqrt{Q_1 Q_2}} \qquad \text{------Eq. 2.24}$$

2.5.3 Analysis

1) How to achieve high efficiency

Firstly, consider coupling efficiency η_{link}. Eq. 2.20 shows that greater k, Q_1, Q_2 will gain higher η_{link}. Optimising k has been done by choosing coil sizes. Now consider how to achieve high Q_1 and Q_2. From Eq. 2.4, Eq. 2.5, Q_1 and Q_2 in Eq. 2.9 can be rewritten as follow:

$$Q_1 = \frac{\Omega L_1}{R_t + R_0} \qquad \text{------Eq. 2.25}$$

$$Q_2 = \frac{1}{\Omega L_2 (\frac{1}{R_r} + \frac{1}{R_{eq}})} \qquad \text{------Eq. 2.26}$$

Once the frequency, the transmitter and the load have been chosen, Ω, R_0 and R_{eq} will be fixed. Only the parameters L_1, R_t, L_2 and R_r left to be determined. In other words, improving Q_1 and Q_2 depends on selecting coil turns and wire gauge.

Increasing the inductance L_1 (or adding more turns to the primary coil) might give a higher Q_1, but it might not always be true because coil series resistance R_t will also increase. Only the $L_1/(R_t+R_0)$ ratio follows the value of Q_1. Similarly, decreasing L_2 (or reducing secondary coil turns) may not always give a higher Q_2, as R_r will decrease too. Only lowering the $L_2(1/R_r+1/R_{eq})$ ratio will result in a higher Q_2.

As to overall efficiency $\eta_{overall}$ in Eq. 2.22, not only is the ratio of inductance to resistance important, but also the ratio between the resistances, R_{eq}/R_r. Greatest k and Q_1 are still expected to give higher $\eta_{overall}$, but greatest Q_2 may not be desirable. Although it makes η_{link} higher so that the secondary circuit gains more power as a whole, the real usable power to R_{eq} may actually decrease.

The above analysis shows that in designing a link with high efficiency, the transmitter coil parameters can be chosen independently: the goal is to achieve high Q_1. When selecting receiver coil parameters, however, one has to see the combined effect by

η_{link} and $\eta_{receiver}$. It is not obvious. Here, the method is to select several possible coils, plot the efficiency of all choices, then compare and select the best. A design example will be given later.

2) **How to achieve good displacement tolerance**

The voltage gain is most stable around the critical coupling. Hence, achieving a good displacement tolerance is down to setting the value of the critical coupling, to making it somewhere in the middle of the working k range. Eq. 2.24 shows that critical coupling is the function of Q_1 and Q_2. Therefore, as before, the proper transmitter and receiver coil parameters have to be chosen.

It is possible that coil parameters selected for good efficiency sometimes happen to produce a desirable critical coupling coefficient, but sometimes do not. In the literature, it was believed that the efficiency and displacement tolerance always conflict with each other [28, 100, 110]. From the author's observation, however, whether they conflict or not depends on which range of the k the system works in. As a general prediction, when the working of the k range decreases, the chances that they are optimised simultaneously increase. For a link working in the range of $k \approx 0.1 \sim 0.5$, optimising displacement tolerance has to sacrifice the efficiency. For a link working in the range of $k \approx 0.01 \sim 0.1$, the two are approximately close. When $k < 0.01$, the position of critical coupling is convergent with the position for good overall efficiency, but it is less likely to happen in a practical case. It is because, in practice, Q_1 and Q_2 cannot be infinitely large, so the possibility for the critical coupling being less than 0.02 is small. So, only in a region of $k \approx 0.01 \sim 0.1$, can efficiency and placement tolerance be made approximately optimal simultaneously. It is the region where the critical coupling method could be most effective and this is the case for the system discussed in this thesis, whose typical working value of k is around $0.03 \sim 0.06$.

Therefore, in designing such a system, the coil parameters can be selected initially from the efficiency point of view, and then using the gain versus k diagram to verify the selection.

2.5.4 A design example

1) **Predetermined circuit constraints**

Operating frequency: 4 MHz

Transmitter: Class D, using N-FET (BS170[2]) at the output stage, which makes $R_0 = 5.1\Omega$.

Load at implant: provisionally, the implant power consumption is estimated as 3mA at 3.3V. So $R_{eq} = ½ (3.3/0.003) = 550\ \Omega$

2) **Choosing possible coils**

As discussed, having more turns for the primary coil might result in a high Q_1, but on the other hand, when the coil series resistance R_t becomes too large, Q_1 falls. To avoid the stray capacitances significantly detuning the resonant frequency, it also requires the coil inductances not to be too great so that their corresponding tuning capacitances will not be too small. Therefore, the transmitter coil can be chosen from the following coils:

12 turns /0.25mm, 8 turns /0.25mm, 8 turns /0.375mm, 6 turns/ 0.5mm.

Fewer turns for the receiver coil are likely give higher Q_2, so we start from the small number of turns. Possible receiver coils are:

2 turns 0.5mm, 4 turns/0.5mm, 4turns/0.375mm, 8turns/0.25mm.

3) **Choosing the transmitter coil**

Choosing the transmitter coil focuses on selecting a coil with highest Q_1.

In Table 2.1, the inductance and the serial resistance of the possible transmitter coils at f_0 = 4 MHz are taken from Donaldson & Perkins's measurement [28]; the corresponding Q_1 is calculated according to Eq. 2.25. It shows 12 turns/0.25 mm is the choice.

[2] Philps semiconductor.

Table 2.1 Transmitter coil parameters

Transmitter parameters (L_1)	L_1(μH)	R_t (Ω)	$Q_1 = \frac{\Omega L_1}{R_t + R_0}$
12 turns 0.25mm	19.9	4.35	53
8 turns 0.25mm	9.69	2.47	32.1
8 turns 0.375mm	8.75	1.86	31.6
6 turns 0.5mm	4.84	0.92	20

4) **Choosing the receiver coil.**

The decision will be based on the efficiency versus k and the gain versus k plots. In Table 2.2, the inductance and serial resistance of those possible receiver coils at $f_0 = 4$ MHz are also taken from Donaldson & Perkins's measurement; the corresponding Q_2 is calculated according to Eq. 2.26; receiver efficiency $\eta_{receiver}$ is calculated from Eq. 2.21.

Table 2.2 Receiver coils parameters

Receiver L_2 parameters	L_2 (μH)	R_r (Ω)	$Q_2 = \frac{1}{\Omega L_2(\frac{1}{R_r} + \frac{1}{R_{eq}})}$	$\eta_{receiver}$
2 turns 0.5mm	0.48	900	28	0.621
4 turns, 0.5mm	1.64	4000	12	0.879
4turns, 0.375mm	1.76	3500	11	0.864
8turns, 0.25mm	6.76	15000	3	0.964

Each receiver coil is then paired with the chosen transmitter coil. Corresponding η_{link} and $\eta_{overall}$ versus k are calculated from Eq. 2.21 and Eq. 2.22. The voltage gain A is calculated from Eq. 2.23. Find the A_{max} and the A/A_{max} using Matlab[3]. A/A_{max} is the normalised gain. The results are plotted in Fig. 2.5.

[3] Version 6.0, release 12. The MathWorks, Inc.

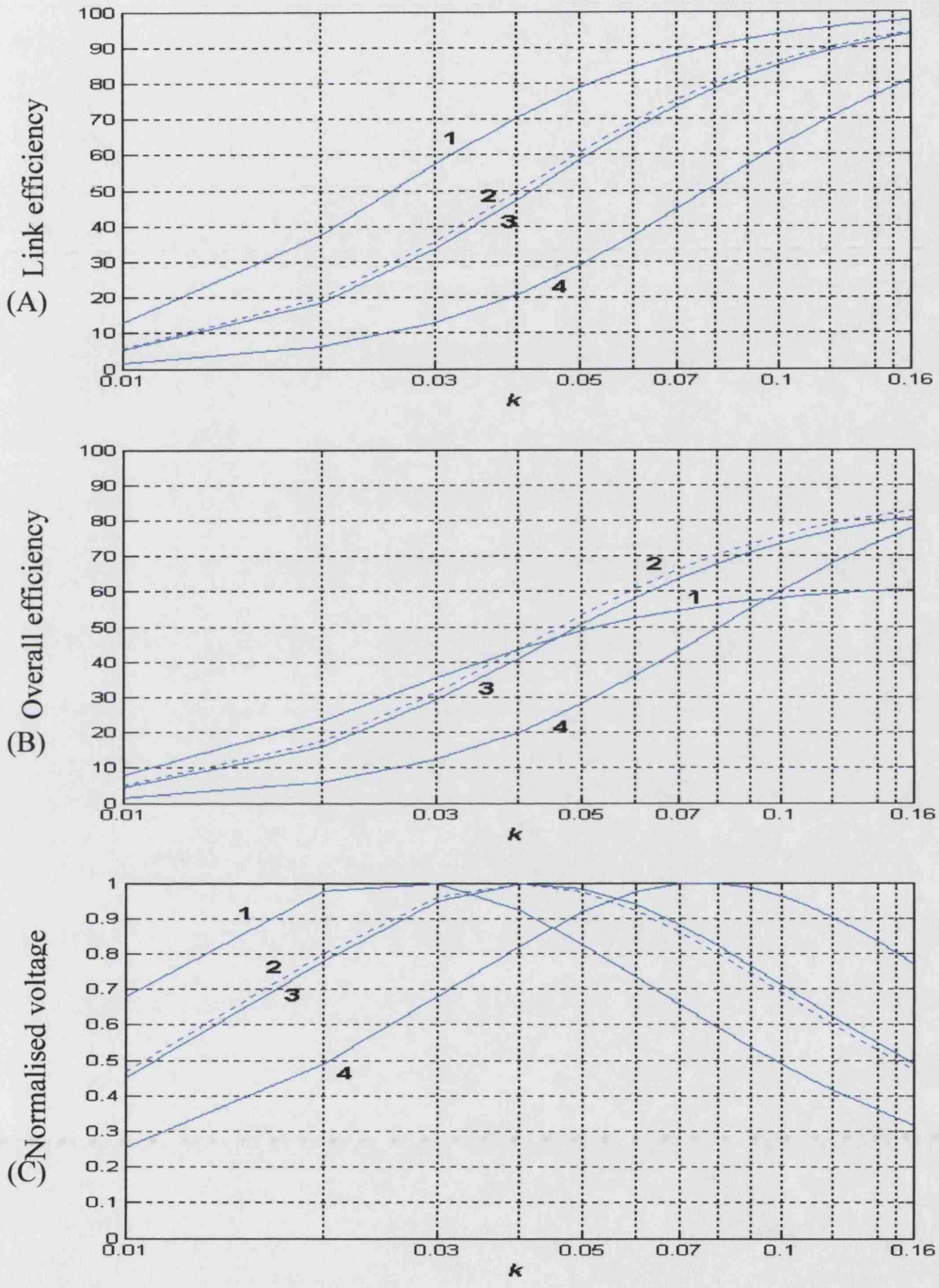


Fig. 2.5 η_{link}, $\eta_{overall}$ and the normalised voltage gain.

Transmitter coil: 12 turns /0.25mm. It is paired with 2 turns /0.5mm receiver coil -- curve 1; with 4 turns/0.5mm receiver coil -- curve 2; with 4turns/0.375mm receiver coil curve 3; with 8 turns/0.25mm receiver coil -- curve 4.

In Fig. 2.5 (A), curve 1 gives the best link efficiency. However, in Fig. 2.5 (B), the overall efficiency of curve 1 is much more reduced due to low $\eta_{receiver}$ (see Table 2.2). Although still being higher at the low value of k, it is worse when $k > 0.05$. On the other hand, curve 2 performs better over a whole range of k. Fig. 2.5 C also shows curve 2 has best displacement tolerance. Therefore the corresponding receiver coil 4 turns/0.5mm is chosen.

The component values for Fig. 2.3 are listed in the following table:

Table 2.3 Component values for the optimal RF power link

Transmitter circuit	Receiver circuit
Coil: 60mm diameter, 12 turns/0.25 mm.	Coil: 45 mm diameter, 4 turns/0.5mm
$R_1 = 9.45\ \Omega$ ($[R_0 = 5.1\ \Omega] + [R_t = 4.35\ \Omega]$)	$R_2 = 483\ \Omega$ ($R_r = 4000\ \Omega$ // $R_{eq} = 550\ \Omega$)
$L_1 = 19.9\ \mu H$	$L_2 = 1.64\ \mu H$
$C_1 = 79.6$ pF	$C_2 = 966$ pF

By Eq. 2.9, the above table gives the quality factors for the primary and the secondary circuit, there are

$$\left.\begin{array}{l} Q_1 = 53 \\ Q_2 = 12. \end{array}\right\} \quad \text{------ Eq. 2.27}$$

2.6 Typical circuit parameters in the RF power link

As analysed above, the value of Q_1 is affected by the output resistance of the power transmitter and by the primary coil resistance. In RF link designs, it is usually in the range 30 ~ 100. Q_2 is affected by the load in implant and by the secondary coil resistance. Assuming the stimulator electronics in the implant is switched off while recording, the load would be moderate, Q_2 is hence estimated around 10 ~ 30. Table 2.4 lists the typical circuit parameters for a moderate range RF link. They will be cited later.

Table 2.4 Typical circuit parameters for a moderate range RF link.

k: 0.01 ~ 0.16
Q_1: 30 ~ 100
Q_2: 10 ~30

2.7 Phase relations

Phase relations of signals v_s, i_1, v_{C1}, i_2 and v_{C2} are denoted by Eq. 2.12, Eq. 2.14, Eq. 2.16 and Eq. 2.18. They are rewritten here and are illustrated in Eq. 2.6.

$$\angle Vs = 0$$

$$\angle I_1 = Arc\tan\left(\frac{1}{\frac{1}{k^2 Q_1} + Q_2}\right)$$

$$\angle V_{C1} = \angle I_1 - \frac{\pi}{2}$$

$$\angle I_2 = \angle I_1 + Arc\tan(Q_2)$$

$$\angle V_{C2} = \angle I_1$$

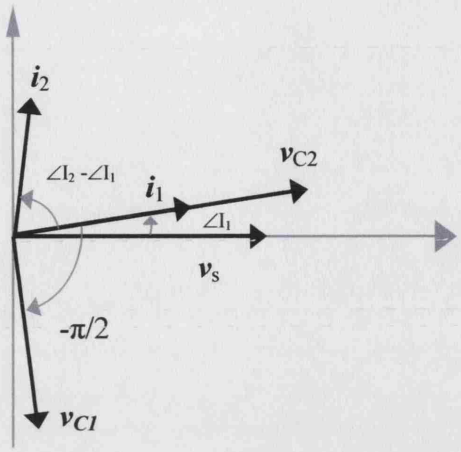


Fig. 2.6 The signal phase relations.

Fig. 2.6 shows that relative to i_1, v_{C1} is always quadrature delayed, v_{C2} is always in phase, i_2 has $\angle I_2 - \angle I_1$ phase in advance, but it depends solely on Q_2. Compared to v_s, i_1 has a phase advance of $\angle I_1$ which is the function of k, Q_1, Q_2.

Given typical circuit parameters as in Table 2.4, the range of $\angle I_1$ and $\angle I_2 - \angle I_1$ can be estimated using Matlab, plotted in Fig. 2.7 and Fig. 2.8.

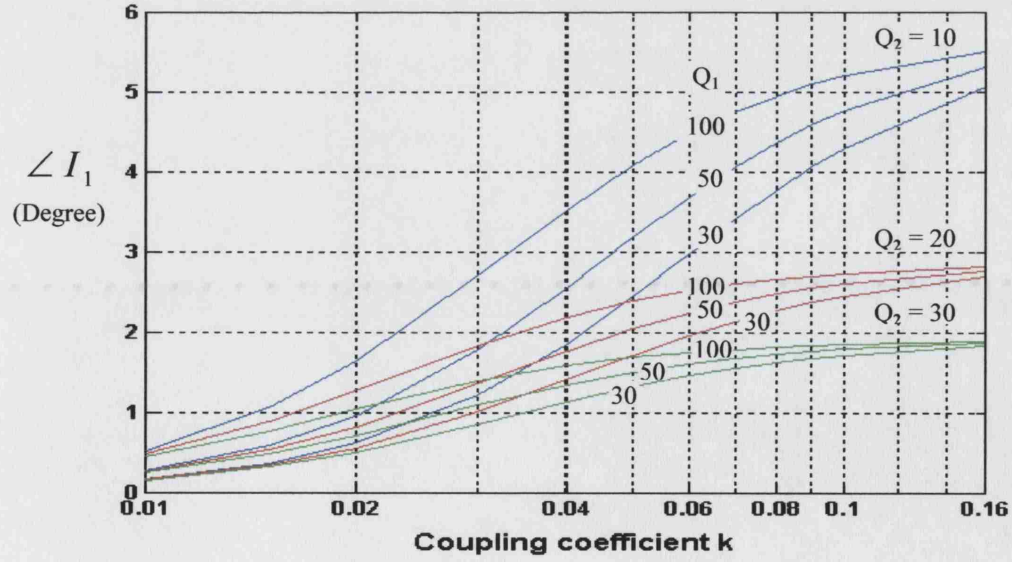


Fig. 2.7 The range of $\angle I_1$

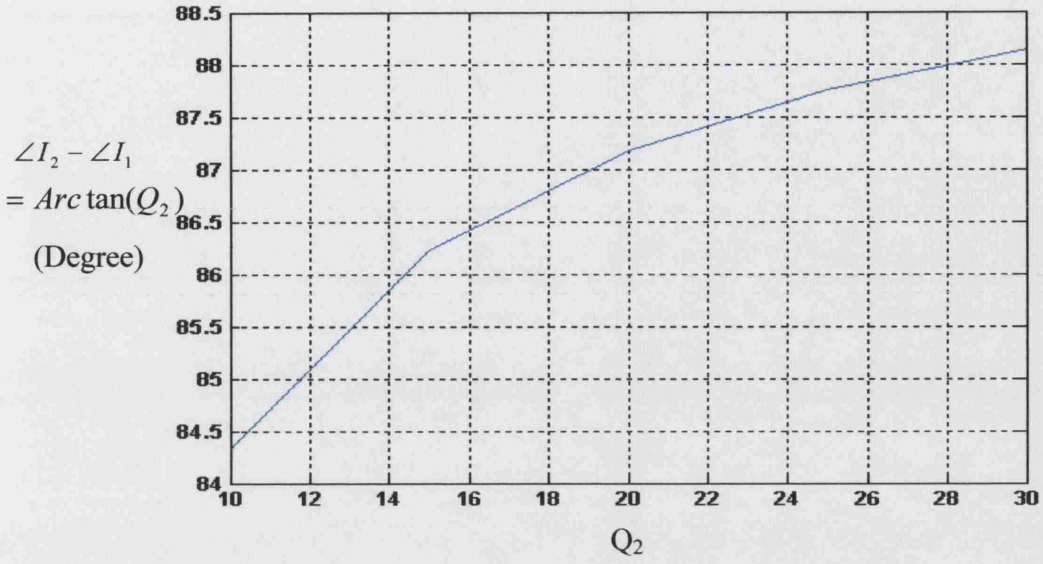


Fig. 2.8 The range of $\angle I_2 - \angle I_1$ or $Arc\tan(Q_2)$.

Fig. 2.7 shows the range of $\angle I_1$ is from 0° to 5.5°, and Fig. 2.8 shows the range of $\angle I_2 - \angle I_1$ is from 84° to 88°. Fig. 2.9 plots an example of the phase relations in the time domain when $Q_1 = 53$, $Q_2 = 12$, $k = 0.04$.

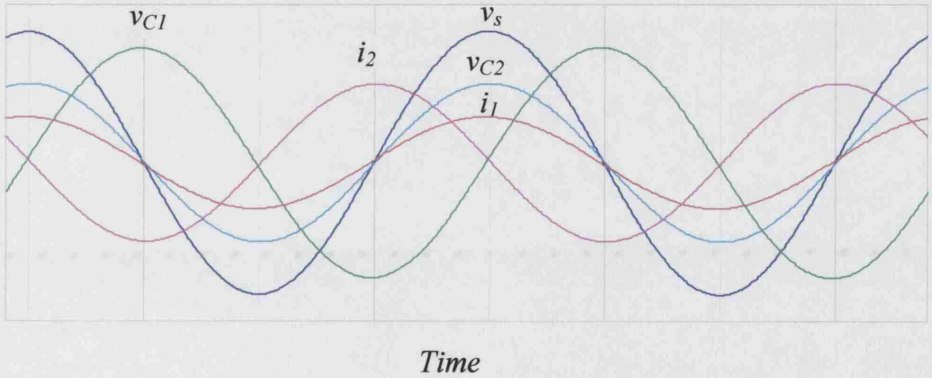


Fig. 2.9 An example of the signal phases in the time domain (amplitudes are not to scale).

2.8 Summary

This chapter discussed the design of an optimised RF power link. The following features have been derived and will be referred to by the later chapters throughout this thesis:

- The circuit configuration for the RF power transmission link, given by Fig. 2.3.
- The optimised component values for the RF link, listed in Table 2.3 or Eq. 2.27.
- The typical range of the circuit parameters in Table 2.4.
- The signal responses in steady-state, by Eq. 2.11, Eq. 2.12, Eq. 2.13, Eq. 2.14, Eq. 2.15, Eq. 2.16, Eq. 2.17 and Eq. 2.18.
- The phase relations in Section 2.7.

In the next chapter, *Passive Phase Shift Modulation* will be introduced.

Chapter 3 Introducing Passive Phase Shift Modulation

3.1 Introduction

This chapter will introduce the principle of *Passive Phase Shift Modulation* (PPSM). As a comparison, the mechanism of *Impedance Modulation* will firstly be addressed, followed by that of PPSM. Two circuit configurations for realising PPSM will be suggested, but only one of which is applicable to a practical system. Comparison between *Impedance Modulation* and PPSM on synchronisation, working distance, energy consumption and speed will be conducted using PSpice simulation[1]. Finally, questions related to further understanding of PPSM will be raised, which will be considered in later chapters. Apart from the mechanism of *Impedance Modulation*, most of these issues have not been discussed before, and they are the author's own contributions.

3.2 Brief background

In a normal RF power transmission, the coupled circuits resonate in a sinusoidal steady-state. However, if any change happens in the secondary circuit, the steady-state will be disturbed, causing variations in the currents and the voltages on both sides. In particular, the primary current i_1(t) and the voltage on the tuning capacitor C_1 (Fig. 2.3 in Chapter 2) can easily be monitored to trace changes in the secondary circuit. Both *Impedance Modulation* and PPSM utilise this feature but use different principles.

3.3 Impedance modulation

Derived from Eq. 2.7 of the last chapter, the relation of the voltage source v_s and the primary current i_1 is

$$E = \left(R_1 + j(\Omega L_1 - \frac{1}{\Omega C_1}) + \frac{(\Omega M)^2}{Z_2} \right) I_1 \qquad \text{------ Eq. 3.1}$$

In which Z_2 is the impedance of the secondary circuit, and there is

[1] Release 9.1, OrCAD, Inc

$$Z_2 = \frac{R_2}{1+\Omega^2 C_2^2 R_2^2} + j\left(\Omega L_2 - \frac{\Omega C_2 R_2^2}{1+\Omega^2 C_2^2 R_2^2}\right) \quad \text{------ Eq. 3.2}$$

Eq. 3.1 shows that the inductively coupled circuits in Fig 2.3 of Chapter 2 have an equivalent circuit shown in Fig. 3.1 which consists of all the components of v_s, L_1, R_1 and C_1 from the primary circuit plus an additional series impedance $\frac{(\Omega M)^2}{Z_2}$. This extra impedance represents the effect the secondary circuit produces on the primary current [97] (page 149).

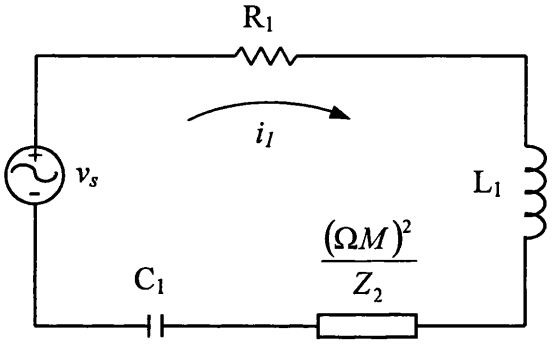


Fig. 3.1 The equivalent circuit of Fig.2.3.

Hence, Eq. 3.1 can be written as

$$\frac{E}{I_1} = Z_{total} \quad \text{------ Eq. 3.3}$$

Where Z_{total} is the total impedance in the equivalent primary circuit,

$$Z_{total} = R_1 + j(\Omega L_1 - \frac{1}{\Omega C_1}) + \frac{(\Omega M)^2}{Z_2} \quad \text{------ Eq. 3.4}$$

If the primary and secondary are both resonant at the operating frequency, which has $\Omega = \frac{1}{\sqrt{L_1 C_1}} = \frac{1}{\sqrt{L_2 C_2}}$, with $M = k\sqrt{L_1 L_2}$, Z_{total} can then be presented as

$$Z_{total} = R_1 + k^2 L_1 \left(\frac{R_2}{L_2} - j \frac{1}{\sqrt{L_2 C_2}} \right) \quad \text{------ Eq. 3.5}$$

Eq. 3.5 shows that any variation of the L_2, C_2, R_2 and coupling coefficient k will change the value of Z_{total}, which in turn will affect both magnitude and phase of the primary current. By deliberately altering these parameters in certain patterns, the modulation in the primary current will occur. In practice, R_2 and C_2 values are easier to modify than L_2, giving *passive resistive load modulation* through R_{mod} [67, 73, 96] or *passive capacitive modulation* through C_{mod} [99] (Fig. 3.2). Therefore, its working principle is modulating the impedance seen by the primary circuit.

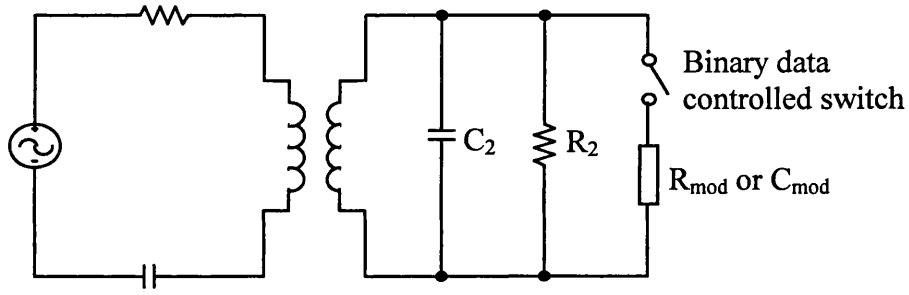


Fig. 3.2 Passive ohmic load modulation or passive capacitive modulation.

3.4 Passive phase shift modulation

3.4.1 Introducing the principle

Physically, the capacitor and inductor are energy storage components. If one of the elements in a LC circuit, for example, the inductor L in Fig. 3.3, has stored energy before the switch closes at instant t = 0, then after t = 0 oscillation will occur due to the energy exchange between L and C.

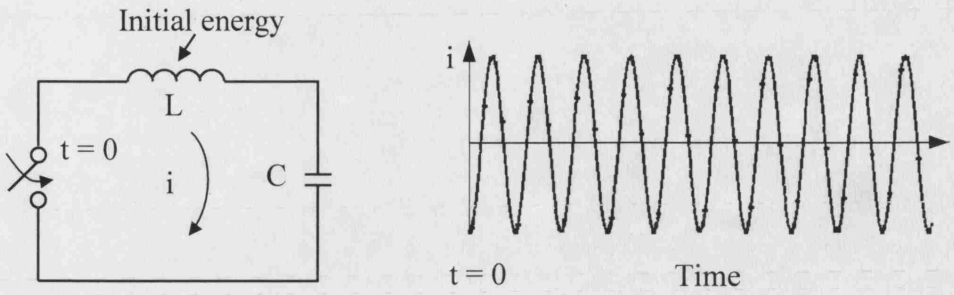


Fig. 3.3 Oscillation occurs after energy in L is released into the LC circuit after t > 0.

If a resistor R is present, the energy will be dissipated in R and the oscillation will diminish (Fig. 3.4). However, if there is a sinusoidal AC source, a steady-state response will be maintained after a transient period during which the pre-stored energy in L is released and is consumed in R (Fig. 3.5).

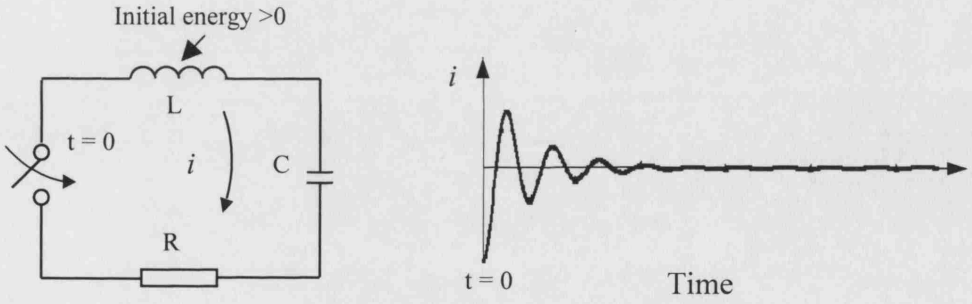


Fig. 3.4 Diminished oscillation in the LRC circuit after t > 0.

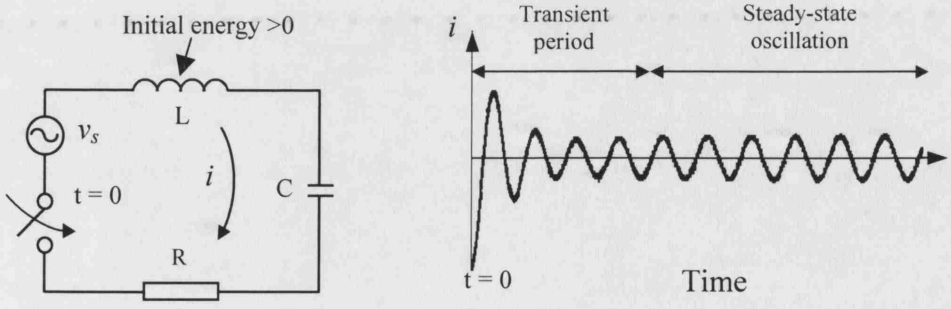


Fig. 3.5 Driven by an AC source, the LRC circuit settles on a steady-state oscillation after a transient period.

The steady state oscillation would carry on forever if there were no disturbance to the circuit. However if at $t = t_1$, extra energy is injected into the circuit somehow, the current amplitude will increase initially and then decay to previous level after the extra energy has been dissipated in R (Fig. 3.6). The amplitude surge marks the event which happened at $t = t_1$.

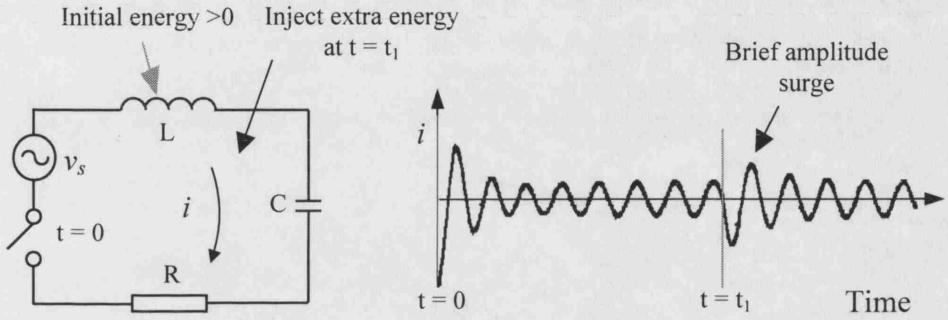


Fig. 3.6 A brief amplitude increase after injecting energy into the circuit at $t = t_1$.

The same principles apply to the circuit in Fig 2.3 of Chapter 2. Considering the energy distribution during the steady-state: part of the energy circulates between the inductors and capacitors to maintain the resonant, part is consumed by the implant load, and the rest is dissipated into the circuit loss resistances. If there is no disturbance, this state will be maintained, and the currents and the voltages (i_1, v_{C1}, i_2, v_{C2}, etc.) will have constant amplitudes. However, if the energy circulating in the secondary circuit is manipulated somehow to break the system balances, the currents and the voltages will vary accordingly to register the event.

The energy stored in a capacitor is (page 309 of [98])

$$Energy\ in\ capacitor = \frac{1}{2} C v_C^2(t) \qquad \text{-------Eq. 3.6}$$

In an inductor, it is (page 309 [98])

$$Energy\ in\ inductor = \frac{1}{2} L i_L^2(t) \qquad \text{-------Eq. 3.7}$$

In a pair of coupled coils, it is (page 338 [98])

$$\textit{Energy in coupled coils} = \frac{1}{2}L_1 i_1^2(t) \pm M i_1(t) i_2(t) + \frac{1}{2}L_2 i_2^2(t) \qquad \text{-------Eq. 3.8}$$

These formulae show that the capacitor voltage and inductor current define the energy state of a circuit. Therefore, by controlling the current or the voltage in the secondary circuit, the energy stored in L_2 or C_2 (Fig. 2.3) can be held and released at a desired time instant to generate a circuit response. This is the principle of *Passive Phase Shift Modulation* (PPSM). There are two ways to generate PPSM. They are described in the following sections.

3.4.2 Two configurations to achieve PPSM

1) Shorting L_2 terminals (Reversing phase of i_2)

Fig. 3.7 shows the circuit configuration and Fig. 3.8 illustrates the signal responses before and after the modulation (solid line in blue) and signals without modulation (dashed line in red).

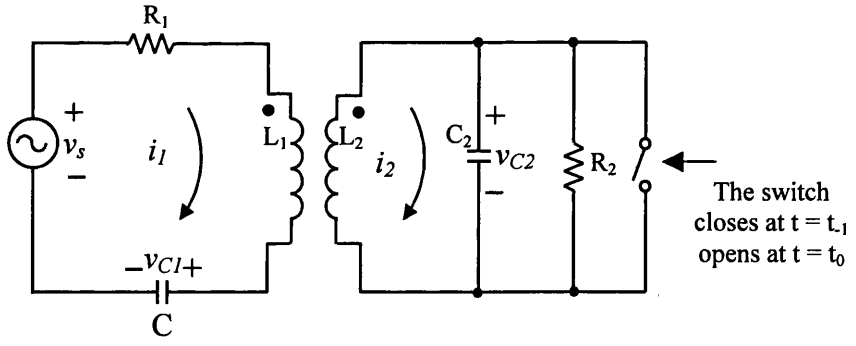


Fig. 3.7 Circuit configuration for reversing phase of i_2 at $t = t_0$.

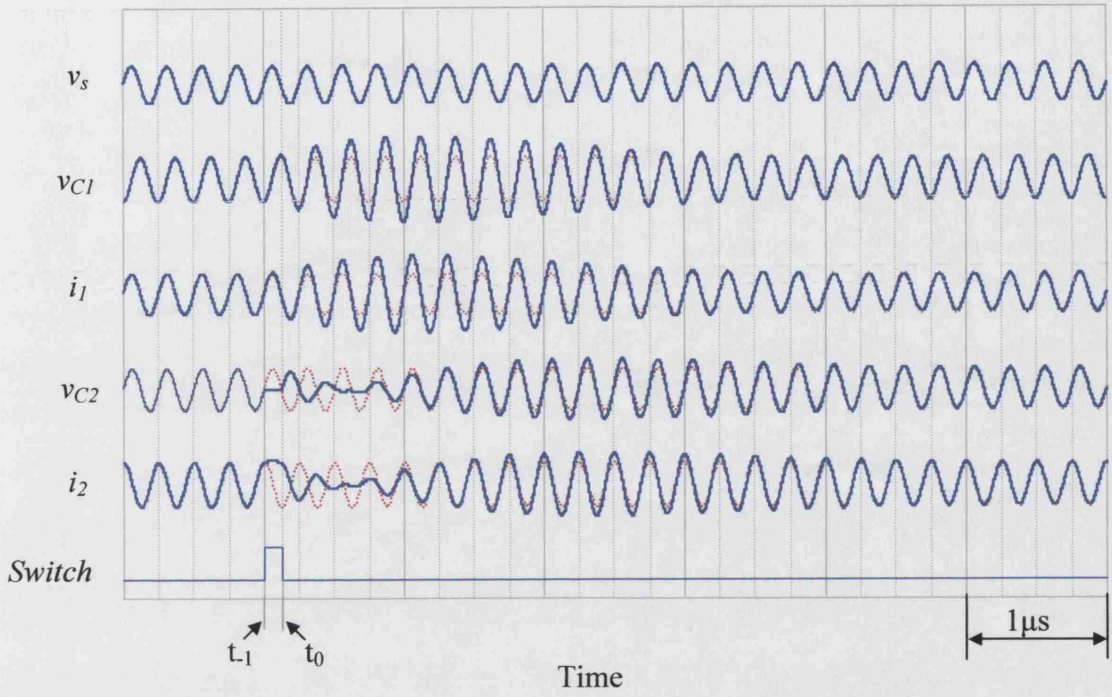


Fig. 3.8 Circuit response of the reversing phase of i_2 by the switch. Signal amplitudes are not to scale. Plotted from PSpice simulation in OrCAD.

The switch closes at $t = t_{-1}$ when the voltage across C_2 (v_{C2}) is passing through zero and increasing positively[2]. Note that the signal phases in this thesis are referred to the phase of the voltage source $v_s = E\cos(\Omega t)$. So, at this instant, the phase of v_{C2} is $\angle V_{C2}(t_{-1}) = \frac{3\pi}{2}$. From Eq. 2.16 and Eq. 2.18 of Chapter 2, which are

$$\angle I_2 = \angle I_1 + Arc\tan(Q_2) \text{ and } \angle V_{C2} = \angle I_1,$$

the phase of i_2 at this instant is obtained as $\angle I_2(t_{-1}) = \frac{3\pi}{2} + Arc\tan(Q_2)$, giving the amplitude of i_2 as $i_2(t_{-1}) = I_{2\max}\cos(\frac{3\pi}{2} + Arc\tan(Q_2))$. From Fig. 2.8, we see that, as $Q_2 >> 1$, $Arc\tan(Q_2)$ is close to 90° or π/2. Hence, $i_2(t_{-1})$ is near its maximal value I_{2max}.

[2] t_{-1} can also be at the time when the voltage across C_2 (v_{C2}) is passing through zero and decreasing. The principle is the same, and only the signal directions are reversed.

The switch shorts the two terminals of L_2. If the switch resistance and L_2 loss resistance are small, the current i_2 will not discharge substantially and is retained at the approximate peak value. Therefore, half a period later, at time $t = t_0$, $v_{C2}(t_0)$ and $i_2(t_0)$ are

$$v_{C2}(t_0) = 0$$

$$i_2(t_0) \approx I_{2max}$$

On the other hand, supposing the switch has not been closed at $t = t_{-1}$, then at instant $t = t_0$, i_2 would approximate its *negative* peak, which is $i_2(t_0) \approx - I_{2max}$. This means the switch action makes the amplitude of $i_2(t_0)$ change from $- I_{2max}$ to I_{2max}. Therefore, when the switch opens at $t = t_0$, more energy than usual from L_2 is released into the circuit: part of i_2 charges C_2, part flows into R_2, and the rest injects energy into the primary circuit, causing the transient increase of i_1.

2) **Disconnecting C_2 (Reversing phase of v_{C2})**

The other method to generate PPSM is to change the phase relations between v_{C2} and i_1. Fig. 3.9 shows the circuit configuration and Fig. 3.10 illustrates the signal responses before and after the modulation (solid line in blue) and signals without modulation (dash line in red).

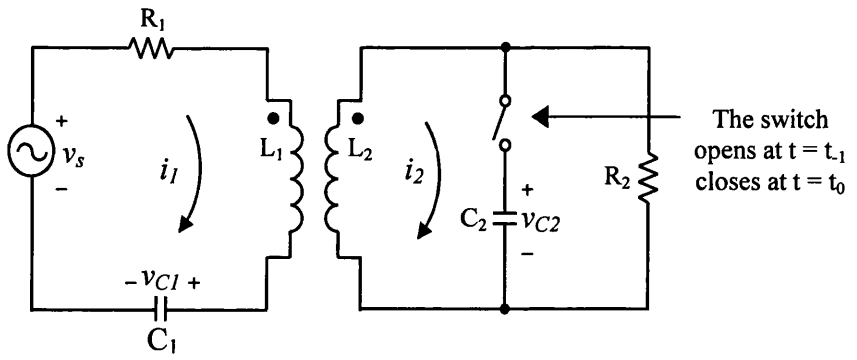


Fig. 3.9. Circuit configuration for reversing phase of v_{C2} at $t = t_0$.

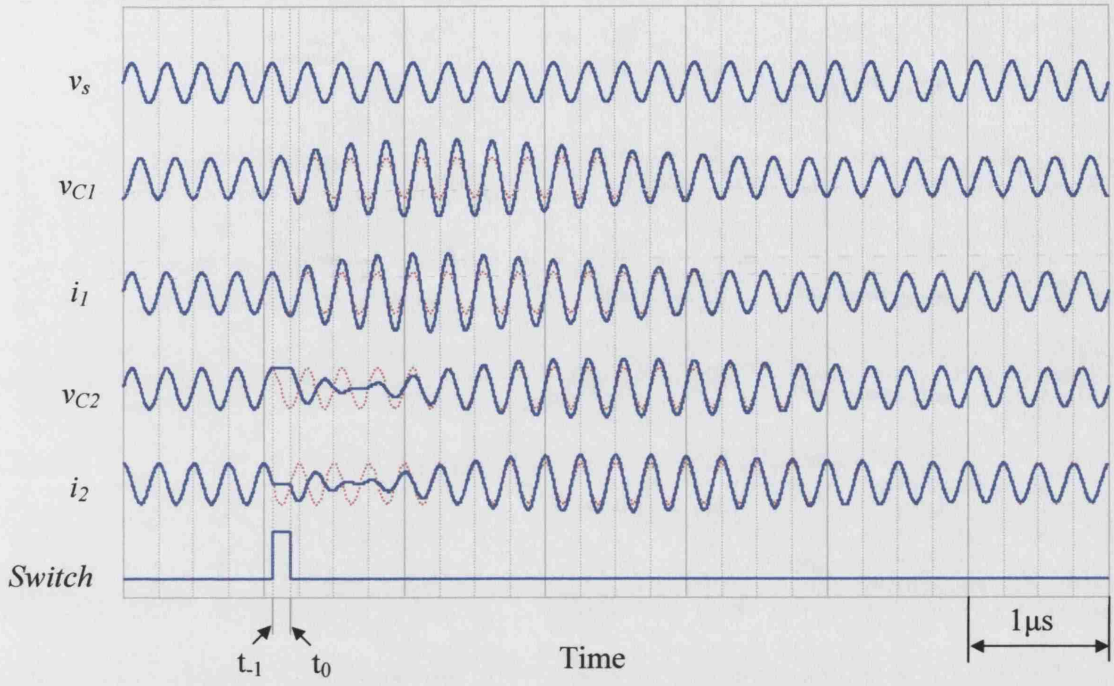


Fig. 3.10 Circuit response of the reversing phase of v_{C2}. Signal amplitudes are not on scale. Plotted from the PSpice simulation in OrCAD.

The switch opens at time $t = t_{-1}$ when the current in L_2 (i_2) is passing through zero and decreasing negatively[3]. At this instant, the phase of i_2 is $\angle I_2(t_{-1}) = \frac{\pi}{2}$. From Eq. 2.16 and Eq. 2.18 of Chapter 2, which are

$$\angle I_2 = \angle I_1 + Arc\tan(Q_2) \text{ and } \angle V_{C2} = \angle I_1,$$

the phase of v_{C2} at this instant is obtained as $\angle V_{C2}(t_{-1}) = \frac{\pi}{2} - Arc\tan(Q_2)$, giving the amplitude of v_{C2} as $v_{C2}(t_{-1}) = V_{C2\,max}\cos(\frac{\pi}{2} - Arc\tan(Q_2))$. As before, $Arc\tan(Q_2)$ is close to 90° or π/2. Hence, v_{C2} is near its maximal value V_{C2max}. The switch disconnects C_2 from the rest of the circuit, holding v_{C2} at its peak. Half a period later, at time $t = t_0$ the signal values become

[3] t_{-1} can also be at the time when the current in L_2 (i_2) is passing through zero and increasing positively. The principle is the same, and only the signal directions are reversed.

$$v_{C2}(t_0) \approx V_{C2max}$$

$$i_2(t_0) = 0$$

On the other hand, supposing the switch has not been opened at $t = t_{-1}$, then at instant $t = t_0$, v_{C2} would be approximately at its *negative* peak, $v_{C2}(t_0) \approx -V_{C2max}$. This means the switch action makes $v_{C2}(t_0)$ change from $-V_{C2max}$ to V_{C2max}. So when the switch closes at $t = t_0$, more energy than usual from C_2 is released into the circuit: part of it then goes to charge L_2, part flows into R_2, and the rest injects energy into the primary circuit, causing the transient increase of i_1.

3.4.3 Comparison of the two configurations

If binary data bits are sent by closing or not closing the switch at regular intervals, amplitude modulation of the primary current i_1 occurs. The switch has the effect of reversing the phase of the secondary coil current i_1 or secondary tuning capacitor voltage v_{C2} and so the method is termed *Passive Phase Shift Modulation* (PPSM). Note that PPSM scheme transmits phase shift modulation, but results in amplitude modulation in the primary current.

In a practical system, the switch may be realised by an FET which always has inherent turn on and turn off resistance R_{on} and R_{off}. R_{on} is normally less than a few ohms and R_{off} is very large. In the first method (shorting the L_2 terminals), the switch opens for most of the time. During this period, it is R_{off} in parallel with R_2. As long as R_{off} is large enough compared to R_2, the circuit will not be affected significantly. By contrast, in the second method (disconnecting the C_2), the switch closes for most of the time. Fig. 3.11 shows the equivalent circuit of Fig. 3.9 when the switch is closed but not ignoring R_{on}. R_{on} is in series with C_2. Although it is only a few ohms, it could cause substantial energy loss during power transmission. Therefore, PPSM by the first method, reversing the phase of i_2, is the applicable option.

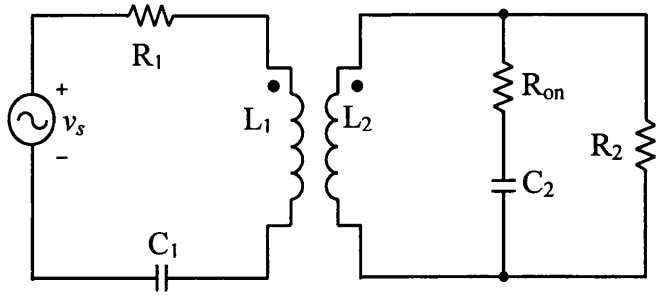


Fig. 3.11 Equivalent circuit of Fig. 3.9 when the switch is closed and its on- resistance R_{on} is not ignored.

3.5 Comparison of *Impedance Modulation* and PPSM

In the following sections, *Impedance Modulation* and PPSM will be compared on synchronization, working distance, energy efficiency and data rate. The comparison is actually among three modulation methods because within *Impedance Modulation*, *load modulation & capacitive modulation* behave differently. It will be conducted using PSpice simulation.

3.5.1 Setting the simulation parameters

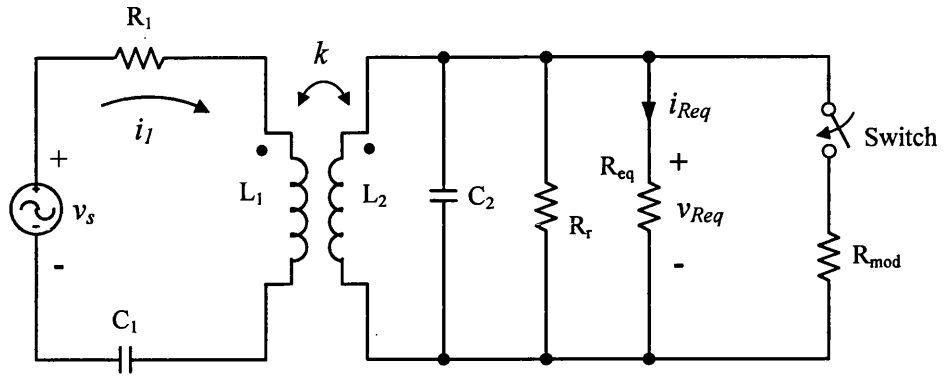
Fig. 3.12 illustrates the circuits used in the simulation. Component symbols and values are the same as those obtained in the optimal design in Table 2.4 of Chapter 2, except R_{mod} and C_{mod} which in this chapter are dedicated only to *load modulation* and *capacitive modulation*. Note that in Fig. 3.12, R_r and R_{eq} are represented individually instead of their summarised form R_2. Rewritten, the values are

Table 3.1 Component values used in the simulation

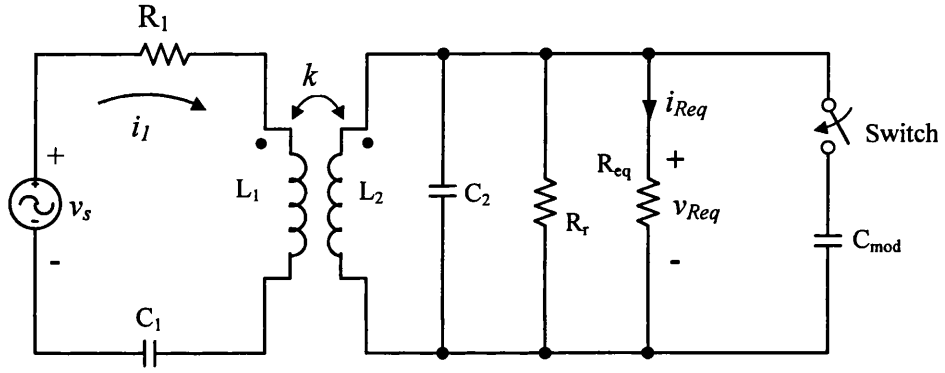
Operating frequency f_0 = 4 MHz, ks are discrete intervals between 0.01 and 0.16	
R_1 = 9.45 Ω	R_r = 4000 Ω, R_{eq} = 550 Ω
L_1 = 19.9 μH	L_2 = 1.64 μH
C_1 = 79.6 pF	C_2 = 966 pF

Selection of the values for R_{mod} and C_{mod} depends on how the comparison standard is set. Here, it is set that all types of modulation should generate equal modulation amplitude of i_1 at $k = 0.1$. So, the procedure for selecting R_{mod} and C_{mod} is as follows:

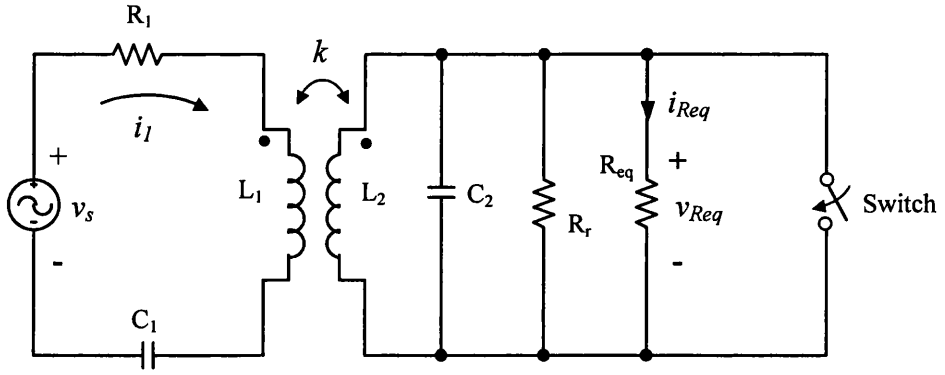
Firstly, assign $k = 0.1$ in Fig. 3.12 (C), run a simulation of the PPSM, record maximum modulation amplitude of i_1; Secondly, substitute this i_1 amplitude into Eq. 3.3 to find Z_{total} for the corresponding *Impedance Modulation*; Thirdly, substitute Z_{total} and all the component values except R_r and R_{eq} in Table 3.1 into Eq. 3.5, and calculate R_2. When *Load Modulation* takes place, R_2 is equal to R_r, R_{eq} and R_{mod} in parallel. While R_r and R_{eq} are already known (see Table 3.1), R_{mod} can be found, which is $R_{mod} = 252\ \Omega$. Similarly, to determine C_{mod} for *Capacitive modulation*, substitute Z_{total} and all the component values except C_2 in Table 3.1 into Eq. 3.5, and then calculate C_2. For easy reference, this C_2 is denoted as C_2' representing the total capacitance when *Capacitive Modulation* takes place. C_2' is equal to original tuning capacitance C_2 in parallel with C_{mod}. Original tuning capacitance C_2 is already known in Table 3.1, so C_{mod} is found, $C_{mod} = 168$ pF. The chosen R_{mod} and C_{mod} will then generate the same modulation amplitude on i_1 at $k = 0.1$ as PPSM does.



(A) *Load modulation*



(B) *Capacitive modulation*



(C) PPSM

Fig. 3.12 The circuits used in the simulation for comparison of the Impedance Modulation and the PPSM.

The other comparison standard to be set is the switch closure duration τ. As has been shown, τ in PPSM is half a RF cycle, equal to 125 ns if the RF frequency is 4 MHz; in the other two modulations τ is chosen that allows i_1 to just reach its maximum value at $k = 0.1$, in other words, let i_1 just reach a new steady-state. Found by iterative procedures in the simulation, for *Load Modulation* τ = 6 μs; for the *Capacitive Modulation* τ = 3.7 μs. Corresponding i_1 waveforms from the three modulations are shown in Fig. 3.13.

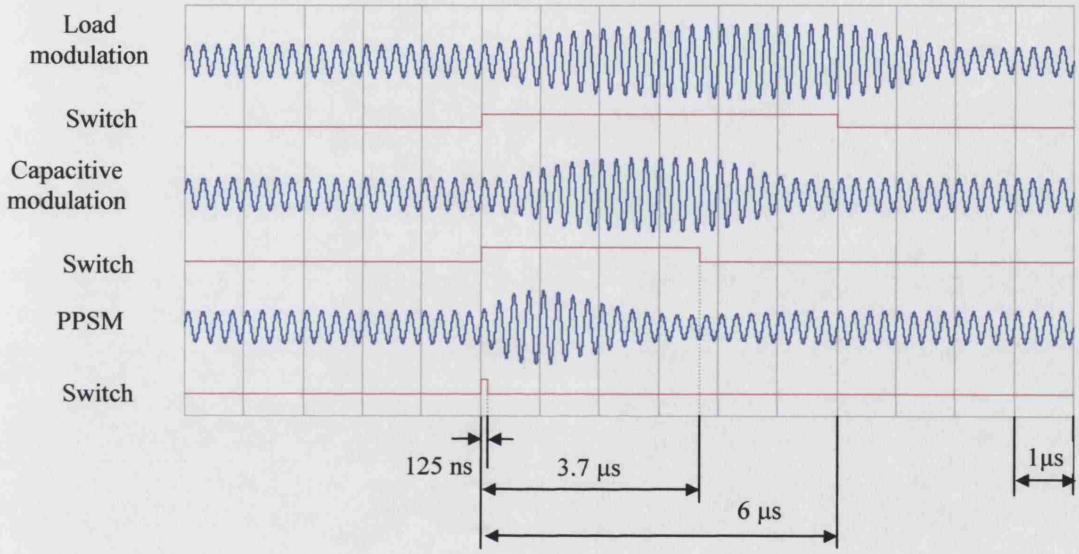


Fig. 3.13 Setting the switching durations for three typse of modulation.

Therefore, the additional parameters used in the simulations are summarised in Table 3.2. From now on, without further notice, the simulation parameters are as those in Table 3.1 and Table 3.2.

Table 3.2 Additional parameters used in the simulations

Load modulation	Capacitive Modulation	PPSM
$R_{mod} = 252\ \Omega$ Switching duration τ = 6 μs	$C_{mod} = 168$ pF τ = 3.7 μs	τ = 125 ns, the switch pulse starts when v_{C2} crosses 0 to go up positively.

3.5.2 Comparing the effect of synchronisation

This section examines how synchronised switching will affect the modulation waveforms in the three types of modulation.

1) **Method**

For convenience, all synchronisations refer to the phase of v_{C2}. Fig. 3.14 shows two cycles of it. The period is 250 ns. Along the *time* axis, t_a is the point when the v_{C2} crosses 0 starting to go up positively, t_b, t_c, t_d and t_e are ¼, ½, ¾ and 1 period points respectively. Let each switch pulse in Fig. 3.13 start or stop at those positions, run the simulations, and record i_1. Compare all the waveforms.

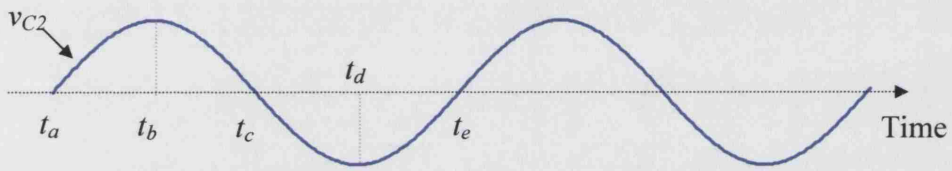


Fig. 3.14 Reference positions on phase of v_{C2}

2) **Results**

In *load modulation* and *capacitive modulation*, when the switching starts and stops has little effect on the amplitude of modulation waveforms as long as the switching duration is equal to or greater than those settings in Fig. 3.13. But for PPSM, the differences are obvious. Synchronised switching which starts from t_a, and stops at t_c (or from t_c to t_e) generates the largest modulation (Fig. 3.15 A); if it starts from t_a, and stops at t_e, the modulation is smallest (Fig. 3.15 C); for any other timing positions, the modulation amplitude is in between (Fig. 3.15, B).

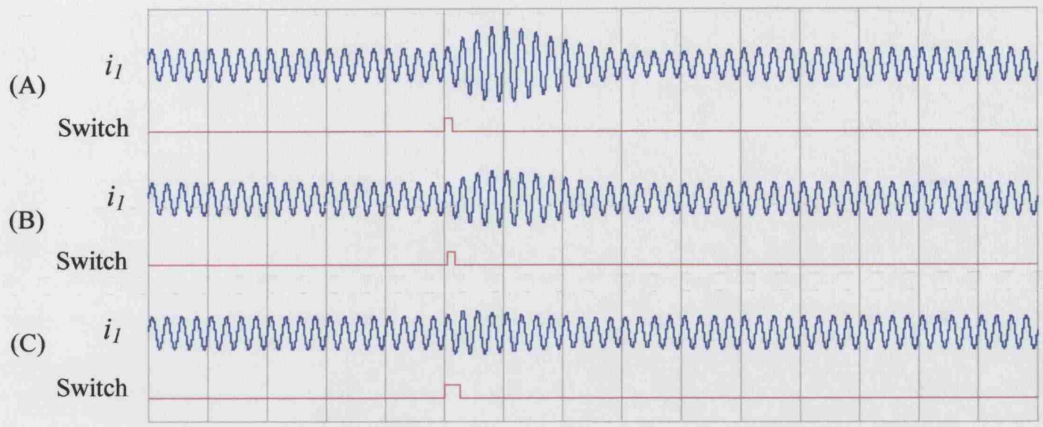
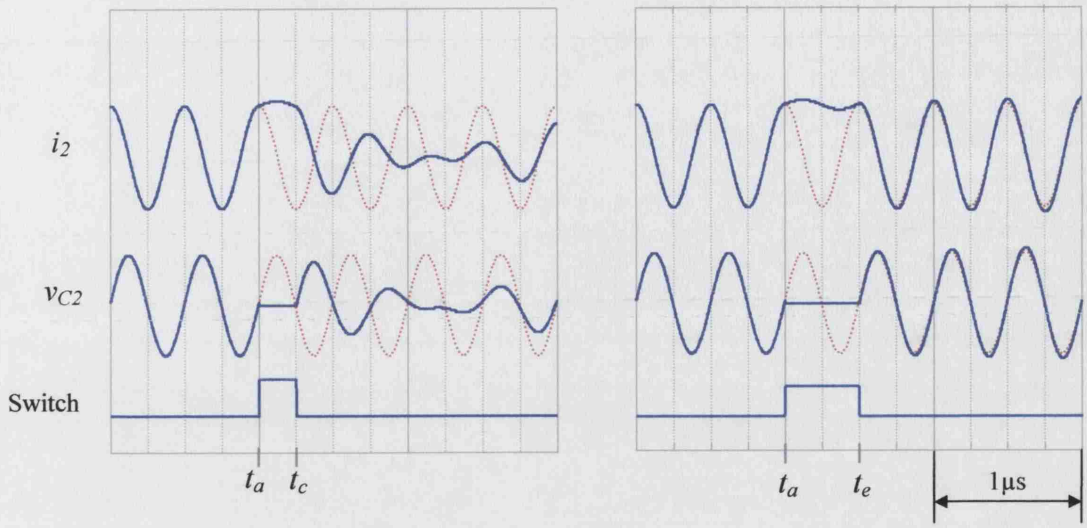


Fig. 3.15 Effect of switching synchronisation on PPSM.

3) **Discussion**

In *load modulation* and *capacitive modulation*, the amplitude of i_1 is determined by the impedance Z_{total}; hence the switch synchronisation does not affect the performance. PPSM, on the other hand, relies on energy storage and release to generate modulation. Controlled by proper timing, maximum energy can be stored and released at the most suitable instant to generate the best impact. Fig. 3.16 shows the enlarged i_2 and v_{C2} at situations in Fig. 3.15 (A) and (C). As before, the solid blue curves are the modulated waveforms, and the red dashed lines are the waveforms if no modulation has occurred. In both situations, the switch is closed at $t = t_a$. It is the time when i_2 is near maximal, so a proximal I_{2max} is kept in L_2 during the switching closure period. If the switch opens at $t = t_c$, as shown in the figure to the left in Fig. 3.16, there will be $2I_{2max}$ more current than usual[4] in i_2 being released into the coupled circuits. But if the switch opens at $t = t_e$, as shown in the figure to the right in Fig. 3.16, no more current than usual[5] in i_2 is released into the coupled circuit. Thus in Fig. 3.15 (A), there is a large increase of i_2; but in Fig. 3.15 (C), the increase in i_2 is very small.

[4] Usual current if there is no modulation at $t = t_c$ is $i_2 \approx -I_{2max}$.
[5] Usual current if there is no modulation at $t = t_e$ is $i_2 \approx I_{2max}$



Situation in Fig. 3.15 (A) Situation in Fig. 3.15(C)

Fig. 3.16 Comparison of switching synchronisation inPPSM.

3.5.3 Comparing the working distance

This section compares the working range among these three modulation types.

1) **Method**

The modulation index indicates the working range. It is calculated by $m = \frac{A-B}{A+B}$, where A is the maximum amplitude; and B is the minimal amplitude. Here, B refers to the amplitude without modulation. Keep the switching duration, start and stop positions as originally settings, run simulations of all three types of modulation at k = 0.005, 0.01, 0.02, 0.04, 0.06, 0.08, 0.1, and 0.16. For each simulation, measure A and B on i_1, calculate m, plot m versus k in Fig. 3.17.

2) **Results**

Fig. 3.17 shows that m in *Load Modulation* and in *Capacitive Modulation* are almost the same at all values of ks. For PPSM, m is greater than the others where $k > 0.1$; smaller where $0.01 < k < 0.1$ and it is almost the same as the others where $k \leq 0.01$.

If m = 0.01 is the minimum value at which the modulation is detectable, then all three types of modulation can work down to k = 0.01. This suggests that their working ranges are comparable.

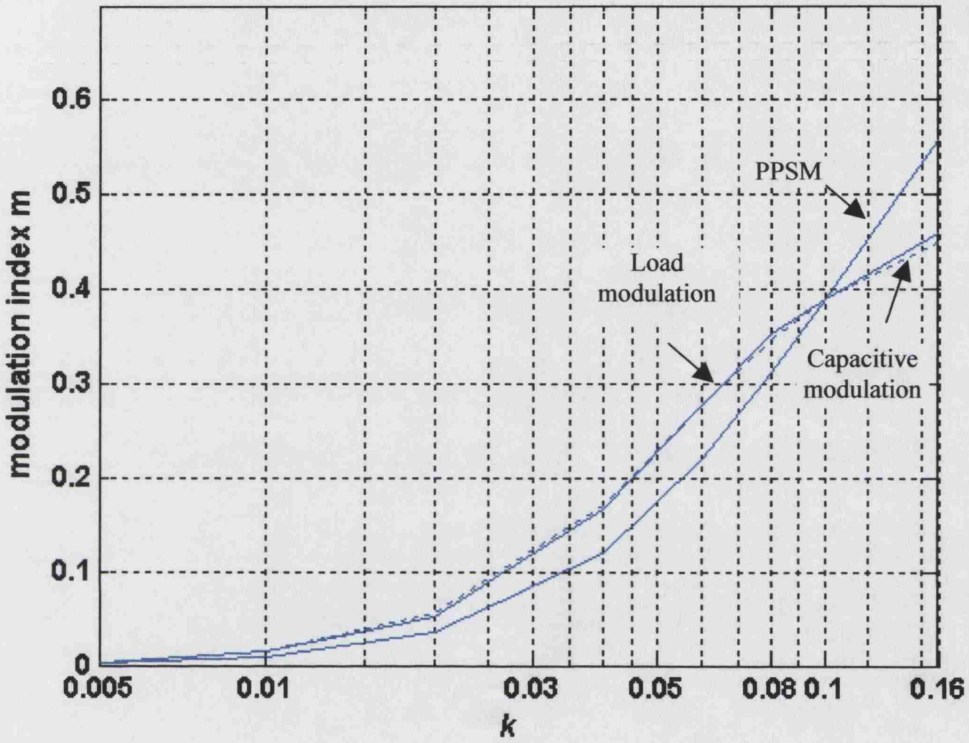


Fig. 3.17 Comparison of the modulation indexes.

3.5.4 Comparing the energy efficiencies

In this section, the overall power transfer efficiencies within one single modulation period are compared.

1) **Method**

The overall efficiency is calculated as the power dissipated in R_{eq} in a period τ' divided by the power output from the source during the same time

$$\eta_{overall} = \frac{P_{Req}}{P_{source}} \qquad \text{------ Eq. 3.9}$$

Where

$$P_{Req} = \frac{1}{\tau'} \int_0^{\tau'} i_{Req}(t) v_{Req}(t) dt \qquad \text{------ Eq. 3.10}$$

$$P_{source} = \frac{1}{\tau'} \int_0^{\tau'} i_1(t) v_s(t) dt \qquad \text{------ Eq. 3.11}$$

$I_{Req}(t)$, $v_{Req}(t)$, $i_1(t)$ and $v_s(t)$ are marked in Fig. 3.12. In the PSpice simulation, these signals are measured at some k values between 0.01 ~ 0.16 and P_{Req}, P_{source} are calculated by the integration over τ' for each modulation type.

τ' is the duration for which the modulation lasts. Note from Fig. 3.13 that it lasts longer than the switching duration τ, so $\tau' > \tau$. Besides, τ' also depends on the coupling coefficient k. To choose proper values of τ' for each type of modulation, the waveforms of i_1 within the range of $0.01 \leq k \leq 0.16$ are examined by running the simulations at the selected k values. The longest duration in each modulation type is selected as τ'. Therefore,

For Load Modulation $\tau' = 10\mu s$

For Capacitive Modulation $\tau' = 9\mu s$

For PPSM $\tau' = 6\mu s$

The results of $\eta_{overall}$ are plotted in Fig. 3.18. As a reference, $\eta_{overall}$ for power transmission only (without modulation) is also plotted in the same figure by the above method. It is compatible with the theoretical result derived in Chapter 2.

2) **Results**

Fig. 3.18 demonstrates that when a modulation occurs, the efficiency decreases. But the amount of reduction varies with the modulation method. PPSM performs better than *capacitive modulation* does and *load modulation* is the worst.

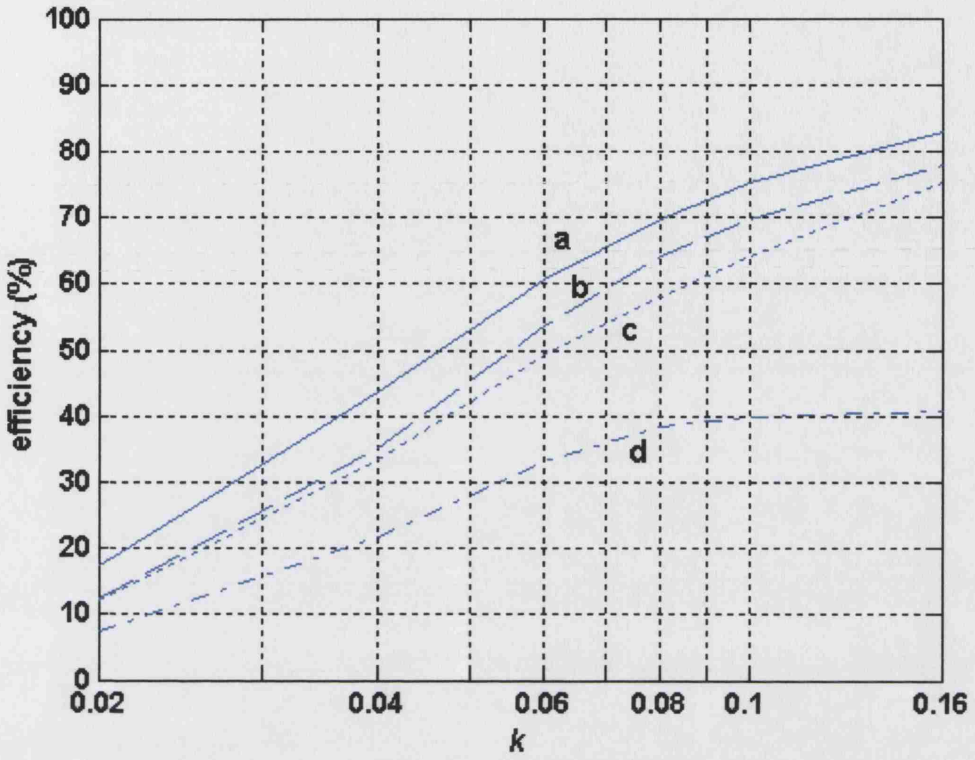


Fig. 3.18 Comparison of the efficiencies. a: no modulation; b: PPSM; c: Capacitive Modulation; d: Load Modulation.

3) **Discussion**

Reduction of the efficiency during the modulations implies that extra power is consumed when transmitting data. In *Load Modulation*, part of the loss is in the primary circuit as the amplitude increase on i_1 results in more I^2R_1; the other loss goes to R_{mod} in the secondary circuit. For *Capacitive Modulation*, the modulation capacitor C_{mod} does not waste any power if it is an ideal component; the same fact applies for the PPSM, where L_2 only stores rather than consumes the energy. So for the last two types of modulation, the reduction in efficiency is mainly due to more I^2R_1 loss in the primary circuit. Therefore they perform better than *Load Modulation*.

From Fig. 3.13, we can see that in *Capacitive Modulation* the waveform shape is flatter than that that in PPSM. It suggests that although the maximal amplitudes are the

same, the average amplitude in *Capacitive Modulation* is greater. Therefore, its I^2R_1 loss is a little higher.

To evaluate the comment that the reduction of efficiency in PPSM is due to increases of I^2R_1, the losses in R_1 are measured when there is no modulation and when there is PPSM in PSpice simulation at the selected k values using the following formulae:

$$\eta_{loss} = \frac{p_{R1}}{P_{source}} \qquad \text{------ Eq. 3.12}$$

Where P_{source} is as Eq. 3.11, and

$$P_{R1} = \frac{1}{\tau'} \int_0^{\tau'} i_1^2(t) R_1 \, dt \qquad \text{------ Eq. 3.13}$$

The loss and overall efficiency for the both cases are plotted in Fig. 3.19.

Let

Increase of the loss in R_1 due to the PPSM
= the $\text{loss}_{\text{with the PPSM}}$ in R_1 – the $\text{loss}_{\text{no modulation}}$ in R_1 ------ Eq. 3.14

Decrease of the efficiency due to the PPSM
= the overall $\text{efficiency}_{\text{no modulation}}$ – the overall $\text{efficiency}_{\text{with}}$ the PPSM ------ Eq. 3.15

By plotting them in the same figure, it shows that the two are equivalent. This suggests that in PPSM, the extra power loss is due to I^2R_1.

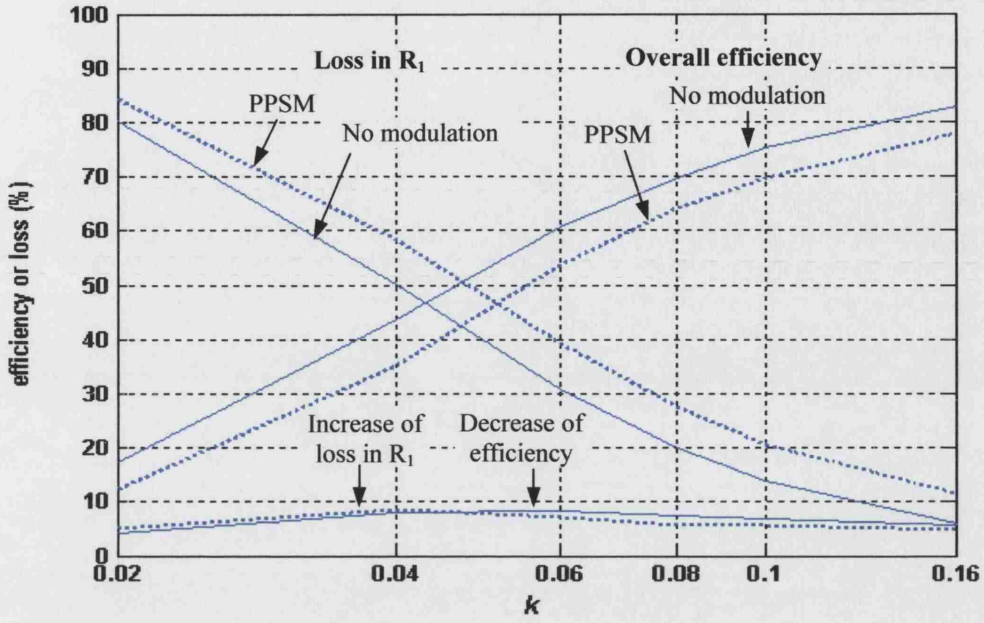


Fig. 3.19 Comparison of the increase in R_1 loss and decrease of overall efficiency.

3.5.5 Comparing the data rate

In *Impedance Modulation* (*Load Modulation* and *Capacitive Modulation*), the modulation waveforms normally have to reach the steady-state. PPSM, on the other hand, works on a transient-state response. Fig. 3.13 demonstrates that the waveform duration for PPSM is much shorter than that in *Impedance Modulation.* Because each modulation is brief, the bits can be sent at shorter intervals, so that a high bit/carrier frequency ratio can be achieved. Because voltage in the implant also recovers quickly, the DC supply to R_{eq} will not be much affected.

One possibility to improve the data rate for *Impedance Modulation* is to shorten the switching time in Fig. 3.12 or Fig. 3.13. However by doing so, the maximal modulation amplitude cannot be achieved, resulting in a shorter coil-coil range. PPSM, on the other hand, can achieve high speed and large coil-coil spacing simultaneously.

3.5.6 Design complexity

Load Modulation is used more often than *Capacitive Modulation.* Its design concentrates on arranging the ratio of the real load and the modulation load in order to reduce power loss [96]. For PPSM, in the implant side, no R_{mod} or C_{mod} is needed. The only requirement is synchronisation; and in the external side, the demodulation design needs attentions for two reasons: 1) the high ratio of bit rate/carrier frequency, 2) the non-uniform modulation waveforms (see later chapters). In general, PPSM design is simpler.

3.6 Summary

PPSM controls energy redistribution to generate modulation. Compared to *Impedance Modulation*, it retains the advantage of using the same carrier for both power and signal transmission while achieving higher data rate, better efficiency and simpler circuit design.

The following hypotheses are tested:

PPSM has advantages in working range, energy efficiency and data rate compared with the conventional *Passive Impedance Modulation.*

The power loss in PPSM is mainly due to the resistive loss in the primary circuit.

They are generally proved to be true except for the claim on working range, which is comparable with that in *Impedance Modulation* rather than outperforming it.

However, PPSM has a transient response. Its behaviour is determined by the circuit's own properties rather than by an outside force. To assist the proper system design, it is necessary to analyse the response in theory, to understand the waveform behaviour, the influence of the circuit parameters and coupling coefficient. In summary, there are several properties to be considered:

1. The function of primary current i_1.

2. How its amplitude is determined.

3. How its duration is determined.

4. How it is affected by the circuit parameters, such as the coupling coefficient and component values.

The next two chapters will be devoted to finding these properties and their implications in the practical system design.

Chapter 4 Analysis of Passive Phase Shift Modulation – Part 1

4.1 Introduction

The aim of the next two chapters is to understand the behaviour of *Passive Phase Shift Modulation* (PPSM) at theoretical level. The mathematical function of the primary current $i_1(t)$ during modulation will be derived. The development of the waveform along k axis and the influence from Q_1, Q_2 will be analysed, and the working range of k, Q_1, Q_2 will be assessed.

As will be seen, the modulation progresses in three stages. This chapter will analyse the first two stages to clarify the initial conditions for PPSM and will discuss the method for solving the circuit response of $i_1(t)$ for stage 3. Developing the mathematical expression of $i_1(t)$ in stage 3 will be presented in the next chapter.

4.1.1 Background

Deriving the mathematical function of $i_1(t)$ of modulation is a problem of finding the transient response for a magnetically coupled circuit including four energy storage components (four modes). Usually, magnetic coupling problems are analysed for a steady-state response, such as in transformer applications for power conversion, signal isolation, impedance matching, and band-pass filters [97, 105] or in neuroprothesis and telemetry applications for RF powering and impedance modulation. The transient response analysis of such problems is rare.

Transient response has been studied for communication networks [43, 105]. However in cases where the net contains three or four more modes (L or C components), the solution becomes appreciably complicated. In these situations, the transient analysis is often either omitted, so the estimation of the net behaviour is based on steady-state solutions alone, or it is much simplified. For example, Weber ([105], p79) derived the symbolic equations by ignoring the resistance, and Guillemin [43] made R, L, and C on both coupling circuits symmetrical.

Passive Phase Shift Modulation relies solely on transient response. Therefore, to characterise the behaviour of $i_1(t)$, transient analysis is inevitable. Furthermore, unlike

the communication networks, the resistances are a significant part of the coupled circuit, and the primary and secondary circuits are often not symmetrical, so that not much simplification can be made, and a mathematical analysis of the modulation has to be developed.

There are several treatments for obtaining a symbolic transient response. Moore [72] introduced Heaviside's operational method; Guillemin discussed the classical approach in great detail [43]; Weber [104, 105] emphasised the Laplace transform method but also presented an extensive review of the classical and operational methods, and gave broad references on each topic; Thomas & Rosa's text book [98] covers almost all the methods. In principle, the goal can be achieved by any of the approaches, but the Laplace transformation is more popular because of being mathematically elegant. In these two chapters, the Laplace transform method will primarily be adopted, but the numerical approach and the classical theory will also be used when it becomes necessary.

4.1.2 Analysis procedure

While the above methods provide general mathematical tools, the analysis procedure has to be designed for this particular problem. There are several steps which are important and are the author's own initiative:

Firstly, the modulation process is identified as having three stages according to the switch position. This divides a complicated problem into three smaller problems.

Secondly, understanding the effect of the switching action on the currents and the voltages helps to establish the initial conditions which cause the modulation. It is done by analysis of the circuit response in stage 2.

Thirdly, in stage 3, there will be several inputs contributing to the transient response of $i_1(t)$. A usual approach is to find the output by each individual source, then sum them to form a complete solution according to the superposition property of the linear circuit. However it is unfeasible here. As we will see, the analysis procedure and the result are already complicated even for a single input, and this usual approach would bury us in a great number of formulae and equations. The author's method is to group

the inputs by their destinations, which will simplify the multi-inputs problem into a single input problem.

Fourthly, after clarifying the inputs or the initial conditions, the main difficulty in deriving the $i_l(t)$ function is that, apart from the substantial amount of labour involved in equation manipulation, at stage 3, there will be a fourth order polynomial that needs to be factorised. Because it has complicated coefficients, factorising symbolically is almost impossible. However, in searching for a solution the author came across Pierce's book [81], in which he solved the problem by a very clever equation manipulation. It also happened that he was studying the transient behaviour of inductively coupled circuits. However in his study, both the primary and secondary coils are series-tuned to a resonant frequency, while the circuit concerned here comprises a series-tuned primary coupled to a parallel-tuned secondary, which is much more complicated. Therefore, his results cannot be directly used for our purpose. Following his steps for equation manipulation, the author derives an analytical solution for our circuit configuration in Appendix 7.

However focusing too much on the pure mathematical process might divert attention from the real physical implications we are trying to understand. Therefore, instead of interpreting a huge symbolic solution from Appendix 7, the author develops another approach, a numerical method, which will arrive at the question-in-concern much more quickly. It will be the method used for the modulation response analysis for stage 3 (see later sections of this chapter and the next chapter).

Fifthly, the waveform shape, duration and amplitude are important characteristics of modulation. They will be analysed while developing the mathematical expression of $i_l(t)$ in the next chapter.

4.1.3 Computer aid tools

In theses two chapters, Mathematica[1] will be used for symbolic equation manipulation; OrCAD[2] will be used for Pspice simulation; and Matlab[3] will be used fornumerical calculation and plotting.

4.1.4 The author's contributions

The author's main contributions in these two chapters are:

1. Developing three important procedures to simplify the analysis: separating the modulation into three stages; proving that the initial conditions for stage 3 can be estimated from the steady-state response; grouping the initial conditions according to their destinations, so turning a multi-input problem into a single input problem.

2. Developing a method to analyse the transient response of the circuit with a higher number of modes and investigating the PPSM in great depth.

3. Uncovering Pierce's method of deriving the analytical solutions for the inductive coupled circuits and, using his method obtaining the analytical solution for the series – tuned primary – parallel tuned secondary circuit configurations.

4.1.5 The physical meanings of the symbols used in the analysis

In these two chapters, and in Appendix 5 and Appendix 7, several symbols appear with different subscripts, namely Ω, Ω_1, Ω_2, Ω', Ω'', ω_1, ω_2, ω_T, ω', ω'', f_0, f_1, f_2, f_{1d}, f_{2d}, f_d', f_d'', α_1, α_2, α_T, α', α'' and $1/\alpha_1$, $1/\alpha_2$, $1/\alpha'$, $1/\alpha''$. Before proceeding with the analysis, their physical meanings need to be clarified and are summarised in Appendix 4. Three current symbols, namely $i_{1\text{steady-state}}$, $i_{1\text{natural}}$ and $i_{1\text{transient}}$, are also used in these chapters. In the following sections, we will see that the behaviour of the circuit during the transient period following the switch opening in stage 3 will be a linear superposition of the steady state and the natural response excited by 2 times the initial secondary current. $i_{1\text{steady-state}}$ represents the steady state response of the primary current, $i_{1\text{natural}}$ is the natural response, and $i_{1\text{transient}}$, is the complete response in the transient period.

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[1] Version 4.1, Wolfram Research, Inc
[2] Version 9.1, OrCAD, Inc.
[3] Version 6.5, copyright 1984-2002, The MathWorks, Inc.

4.2 Three stages during the modulation

Fig. 4.1 is the circuit discussed in Chapter 3 for realising *Passive Phase Shift Modulation.*

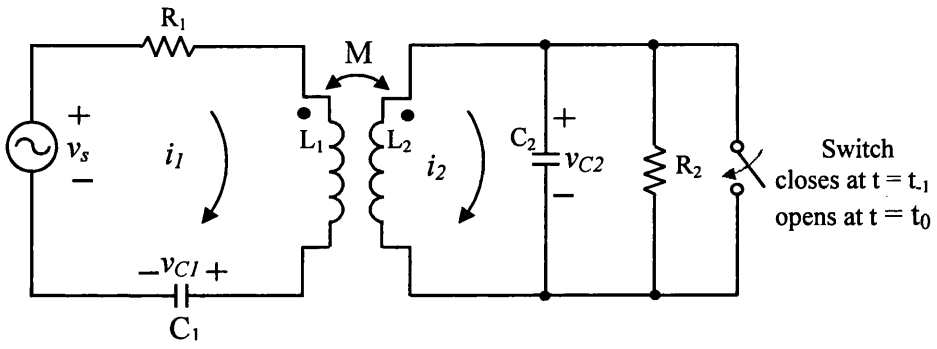


Fig. 4.1 The circuit for realising the PPSM

In a normal power transmission mode, the switch in Fig. 4.1 opens. When a binary '1' needs to be transmitted, at $t = t_{-1}$ the switch closes and at $t = t_0$ it opens again. The switching action divides the modulation process into three stages, and so does the analysis procedure:

Stage 1, when $t < t_{-1}$. The circuit is in normal steady-state. The purpose of solving the signal responses in this stage is to find the status of the external force v_s, the current in L_1 and L_2, and the voltage in C_1 and C_2 at $t = t_{-1}$. They are the initial conditions for stage 2.

Stage 2, during the period of $t_{-1} \leq t < t_0$. The circuit configuration is altered by the switch connection. This period is only half an RF cycle, and the circuit response is in a transient state. From the initial conditions obtained in stage 1, the status of the external force v_s, the currents in L_1 and L_2, and the voltages in C_1 and C_2 at $t = t_0$ are to be found. They form the initial conditions for stage 3.

Stage 3, when $t \geq t_0$. The circuit configuration returns to the status before stage 1. From the initial conditions obtained in stage 2, the transient response of $i_1(t)$ will be found. From the acquired analytical formula, we will know how the waveform is composed, and how to predict the waveform shape, amplitude and duration.

Fig. 4.2 is the summary of the three stages during the modulation. The problems in these stages will be treated in order in the following sections and in the next chapter.

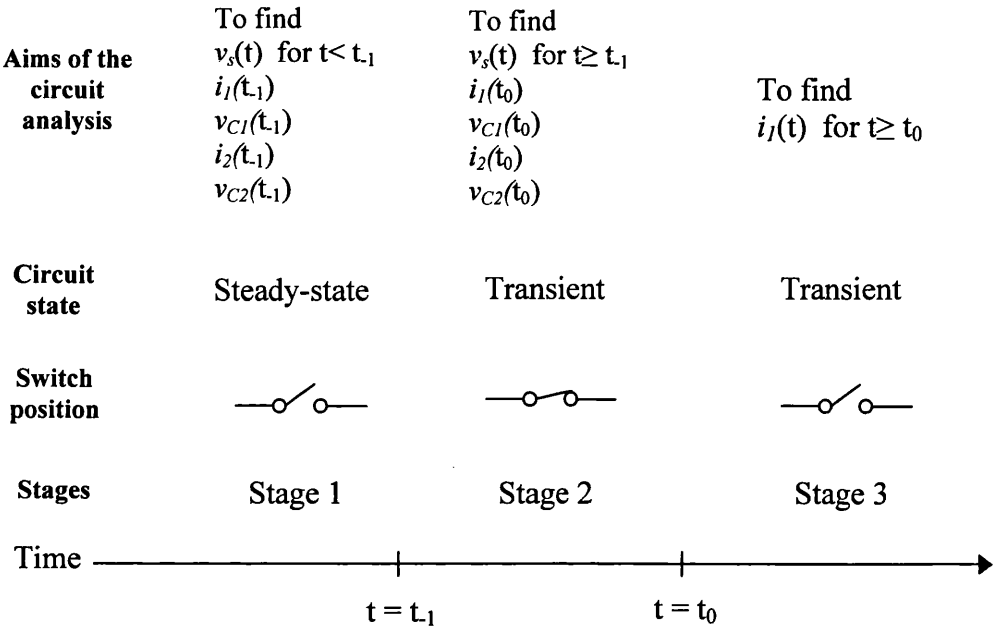


Fig. 4.2 Summary of the three stages during the modulation

4.3 Circuit responses in stage 1 ($t < t_{-1}$) and the initial conditions at $t = t_{-1}$

When $t < t_{-1}$ the responses are in steady-state. They have been derived in section 2.4, Chapter 2. Rewritten in the conventional forms, they are

$$i_1(t) = I_{1\max}\cos(\Omega t + \angle I_1) \qquad \text{------ Eq. 4.1}$$

$$v_{C1}(t) = V_{C1\max}\cos(\Omega t + \angle I_1 - \frac{\pi}{2}) \qquad \text{------ Eq. 4.2}$$

$$i_2(t) = I_{2\max}\cos(\Omega t + \angle I_2) \qquad \text{------ Eq. 4.3}$$

$$v_{C2}(t) = V_{C2\max}\cos(\Omega t + \angle I_1) \qquad \text{------ Eq. 4.4}$$

$$v_s(t) = E\cos(\Omega t)$$ ------Eq. 4.5

The time instant t = t_{-1} is defined as when the voltage on C_2 is passing through zero and increasing positively, so Eq. 4.4 must become

$$v_{C2}(t_{-1}) = 0$$ ------Eq. 4.6

And there is

$$\Omega t_{-1} + \angle I_1 = n\pi + \frac{3\pi}{2},\ n = 0, 2, 4....$$ ------Eq. 4.7

n can be any of these values of { 0, 2, 4 ...} as long as it is consistent from now on. So arbitrarily let n = 0, and rearrange Eq. 4.7. It becomes

$$t_{-1} = \frac{\frac{3\pi}{2} - \angle I_1}{\Omega}$$ ------Eq. 4.8

Substituting t in Eq. 4.1, Eq. 4.2, Eq. 4.3 and Eq. 4.5 with Eq. 4.8, gives

$$\left.\begin{aligned} i_1(t_{-1}) &= I_{1\max}\cos(\frac{3\pi}{2}) \\ v_{C1}(t_{-1}) &= V_{C1\max}\cos(\pi) \\ i_2(t_{-1}) &= I_{2\max}\cos(\frac{3\pi}{2} + \angle I_2 - \angle I_1) \end{aligned}\right\}$$ ------Eq. 4.9

$$v_s(t_{-1}) = E\cos(\frac{3\pi}{2} - \angle I_1)$$ ------ Eq. 4.10

Eq. 4.9 and Eq. 4.10 show that at $t = t_{-1}$, $i_1(t_{-1})$, $v_{C1}(t_{-1})$ and $i_2(t_{-1})$ have the phase angles $\frac{3\pi}{2}$, π and $(\frac{3\pi}{2} + \angle I_2 - \angle I_1)$ respectively; the external sinusoidal voltage reaches the phase angle $\frac{3\pi}{2} - \angle I_1$.

Simplifying Eq. 4.9, it becomes

$$\left.\begin{aligned} i_1(t_{-1}) &= 0 \\ v_{C1}(t_{-1}) &= -V_{C1max} \\ i_2(t_{-1}) &= I_{2max} \sin(\angle I_2 - \angle I_1) \end{aligned}\right\} \quad \text{------ Eq. 4.11}$$

In summary, Eq. 4.6, Eq. 4.10 and Eq. 4.11 are the initial conditions for stage 2.

4.4 The signal values at $t = t_0$ if there were no modulation

For references in the later sections, the would-be signal values at $t = t_0$ if there were no modulation are also found as below:

The duration from $t = t_{-1}$ to $t = t_0$ is half a cycle, or π/Ω. So

$$t_0 = t_{-1} + \frac{\pi}{\Omega}$$

Bringing Eq. 4.8 into above equation, gives

$$t_0 = \frac{\frac{3\pi}{2} - \angle I_1}{\Omega} + \frac{\pi}{\Omega}$$

$$= \frac{2\pi + \frac{\pi}{2} - \angle I_1}{\Omega} \quad \text{------ Eq. 4.12}$$

Substituting t in Eq. 4.1, Eq. 4.2, Eq. 4.3 and Eq. 4.4 with Eq. 4.12, gives

$$i_1(t_0)_{non-modulation} = 0 \quad \text{------ Eq. 4.13}$$

$$v_{C1}(t_0)_{non-modulation} = V_{C1\max} \quad \text{------ Eq. 4.14}$$

$$i_2(t_0)_{non-modulation} = -I_{2\max}\sin(\angle I_2 - \angle I_1) \quad \text{------ Eq. 4.15}$$

$$v_{C2}(t_0)_{non-modulaion} = 0 \quad \text{------ Eq. 4.16}$$

Substituting t in Eq. 4.5 with Eq. 4.12, obtains

$$v_s(t_0) = E\cos(2\pi + \frac{\pi}{2} - \angle I_1) \quad \text{------ Eq. 4.17}$$

4.5 Circuit responses in stage 2 ($t_{-1} \leq t < t_0$) and the initial conditions at $t = t_0$

4.5.1 Circuit configuration

During this stage, the circuit in Fig. 4.1 becomes Fig. 4.3. In a practical situation, the inductor L_2 and switch have series resistance, R_{L2} and R_{on} respectively. R_{sum} in the figure represents their sum, $R_{sum} = R_{L2} + R_{on}$. However it is usually very small. In order to concentrate on fundamental problems and also to simplify the analytical solution, the ideal situation $R_{sum} = 0$ is considered, so Fig. 4.4 will be used in the analysis. The non-ideal (practical) situation when $R_{sum} \neq 0$ will be discussed at the end. Note the resistance R_1 is never ignored.

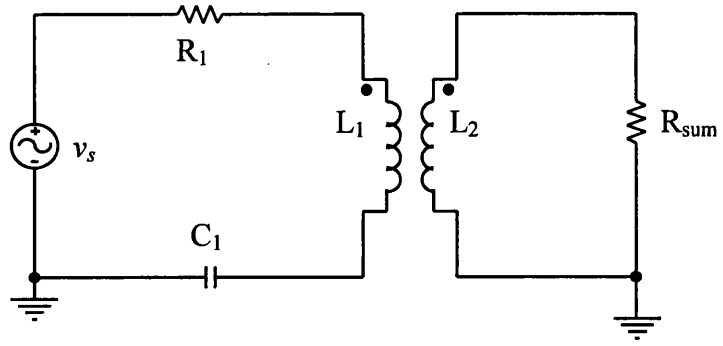


Fig. 4.3 Circuit configuration during $t_{-1} \leq t < t_0$ in the practical situation.

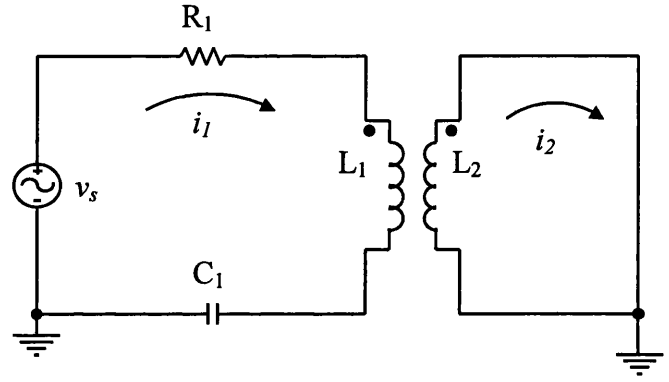


Fig. 4.4 Circuit configuration during $t_{-1} \leq t < t_0$ in the ideal situation.

4.5.2 Circuit responses in stage 2 ($t_{-1} \leq t < t_0$) and initial conditions at $t = t_0$.

With the sign and dot convention in Fig. 4.4, the circuit differential equations are

$$\left.\begin{aligned} R_1 i_1 + L_1 \frac{di_1}{dt} + \frac{1}{C_1}\int i_1 dt - M\frac{di_2}{dt} = v_s(t) \\ -M\frac{di_1}{dt} + L_2\frac{di_2}{dt} = 0 \end{aligned}\right\} \quad \text{------ Eq. 4.18}$$

From the initial conditions given by Eq. 4.6, Eq. 4.10 and Eq. 4.11, we know the non-zero contributions to the circuit response in period $t_{-1} \leq t < t_0$ are from $v_{C1}(t_{-1})$, $i_2(t_{-1})$ and the drive voltage $v_s(t)$. According to the additivity property of linearity circuits, the final response is the sum of the individual responses caused by each input. Therefore, Eq. 4.18 is solved according to this property and by Laplace and Inverse-Laplace

transforms. Because of the complexity, the procedure is described in detail in appendix 5.

Two conclusions have been drawn in appendix 5: firstly, because *the switch closure period is short*, at weak coupling (small *k*), the switch action in the secondary circuit does not significantly affect the primary circuit. $i_1(t)$ and $v_{C1}(t)$ are nearly the same as they would be in the steady-state situation. Hence, $i_1(t_0)$ and $v_{C1}(t_0)$ can be predicted from the steady-state response. So, from Eq. 4.13 and Eq. 4.14, Eq. 4.19 and Eq. 4.20 can be expected. On the other hand, the influence of the primary circuit on the secondary current is also trivial. i_2 is dominated by the DC current, which results from the switch shorting the two terminals of L_2[4]. So $i_2(t_{-1})$ is held until $t = t_0$, and gives Eq. 4.21. Secondly, when the coupling is greater (larger *k*), the influence that the two circuits are on each other is noticeable, even for a short period. However, at $t = t_0$, $i_1(t)$ almost returns to zero, and so does the AC component of $i_2(t)$: hence, Eq. 4.19 and Eq. 4.21 still stand. The value of $v_{C1}(t_0)$ is greater than V_{C1max}, but we can still assign V_{C1max} to $v_{C1}(t_0)$ as in Eq. 4.20, and bear in mind that it represents the worst case; the amplitude of the actual modulation response should be greater.

When $R_{sum} \neq 0$, the secondary current will discharge through R_{sum} during the period of stage 2, so that $i_2(t_0)$ is actually less than $i_2(t_{-1})$. However, R_{sum} is often small, so the effect can be ignored.

The summary of the signal values at $t = t_0$ is

$$i_1(t_0) \approx 0 \qquad \text{------ Eq. 4.19}$$

$$v_{C1}(t_0) \approx V_{C1\max} \qquad \text{------ Eq. 4.20}$$

$$i_2(t_0) \approx i_2(t_{-1}) = I_{2\max}\sin(\angle I_2 - \angle I_1) \qquad \text{------ Eq. 4.21}$$

$$v_{C2}(t_0) \approx 0 \qquad \text{------ Eq. 4.22}$$

and Eq. 4.17

[4] Analogue to the DC voltage held between the terminals of a charged capacitor when its discharging path is disconnected.

Eq. 4.17 shows that at t = t_0, the external sinusoidal voltage arrives at the phase angle $(2\pi + \frac{\pi}{2} - \angle I_1)$. In summary, Eq. 4.19, Eq. 4.20, Eq. 4.21, Eq. 4.22 and Eq. 4.17 are the initial conditions for stage 3.

4.6 Method for solving the circuit response of i_1(t) in stage 3(t ≥ t_0)

4.6.1 Grouping the initial conditions by their destinations

Eq. 4.13, Eq. 4.14, Eq. 4.15, Eq. 4.16 and Eq. 4.17 show that if the circuit were running in steady state to the time instant t = t_0, there would be non-zero signal inputs $v_s(t)$, $v_{C1}(t_0)_{non-modulation} = V_{C1\max}$ and $i_2(t_0)_{non-modulation} = -I_{2\max}\sin(\angle I_2 - \angle I_1)$, where the external source $v_s(t)$ starts from the phase angle $(2\pi + \frac{\pi}{2} - \angle I_1)$. Because of such signal distributions, after t = t_0, the steady state would continue. Therefore, the forces at t = t_0 to keep the coupled circuits running in the steady state are:

v_s(t), v_{C1}(t_0)non-modulation, i_2(t_0)non-modulation

↓ ↓ ↓

v_s(t), V_{C1max} and $-I_{2max}$ sin $(\angle I_2 - \angle I_1)$ ------ Eq. 4.23

Signals at t = t_0 if there were no switching action

Now, return to stage 3. Considering stage 3 is independent from the previous stage, the initial conditions are regarded as inputs to the circuit at t = t_0. There are non-zero contributions to the circuit from $v_s(t)$, $v_{C1}(t_0) \approx V_{C1max}$ and $i_2(t_0) \approx I_{2max}$ sin $(\angle I_2 - \angle I_1)$, where the external source $v_s(t)$ starts from the phase angle $(2\pi + \frac{\pi}{2} - \angle I_1)$. They are written as

$v_s(t)$, $v_{C1}(t_0)$ $\quad$ $i_2(t_0)$

$$Inputs: v_s(t), V_{C1\max} \ and \ +I_{2\max}\sin(\angle I_2 - \angle I_1) \qquad \text{------ Eq. 4.24}$$

Contributions to the complete transient response

Letting $i_2(t_0)$ be the following form:

$$i_2(t_0) = I_{2\max}\sin(\angle I_2 - \angle I_1) = -I_{2\max}\sin(\angle I_2 - \angle I_1) + 2I_{2\max}\sin(\angle I_2 - \angle I_1)$$

and regrouping Eq. 4.24, gives

Inputs:

$v_s(t)$, $v_{C1}(t_0)_{\text{non-modulation}}$, $\quad$ $i_2(t_0)_{\text{non-modulation}}$ $\quad$ $2\times i_2(t_0)$

$v_s(t)$, V_{C1max}, $\quad$ $-I_{2max}\sin(\angle I_2 - \angle I_1)$; $\quad$ and $\quad$ $2I_{2max}\sin(\angle I_2 - \angle I_1)$

------ Eq. 4.25

1st part $\qquad$ 2nd part

Forces for keeping the steady-state $\qquad$ Forces for exciting the natural response

The first part of Eq. 4.25 is the same as Eq. 4.23, which are the forces keeping the circuits running in the steady state; and the second part, $2I_{2max}\sin(\angle I_2 - \angle I_1)$, will produce an excitation called the natural-response. It superimposes itself onto the steady-state response, making a complete transient response. According to the superposition law of the linear circuit, the output is the sum of each output from individual sources. Therefore, in order to find the response for $i_1(t)$, we can find the steady-state response and natural response separately, then add them together. It is

$i_{1transient} = i_{1steady} + i_{1natural}$ ------ Eq. 4.26

4.6.2 Resetting the time origin

The $i_{1steady}$ in the steady state has been solved in Chapter 2, denoted by Eq. 4.1. Substituting t in Eq. 4.1 by Eq. 4.12, and representing $i_1(t_0)$ by $i_{1steady}(t_0)$, gives

$$i_{1steady}(t_0) = I_{1\max}\cos(2\pi + \frac{\pi}{2}) \quad \text{------ Eq. 4.27}$$

Eq. 4.27 shows that at $t = t_0$, $i_{1steady}(t)$ reaches a phase angle $(2\pi + \frac{\pi}{2})$. For convenience, after clarifying all the contributions we now reset stage 3's starting point t_0 as the time origin. $i_{1steady}(t)$ becomes

$$i_{steady1}(t) = I_{1\max}\cos(\Omega t + 2\pi + \frac{\pi}{2})$$

$$= -I_{1\max}\sin(\Omega t) \quad \text{------ Eq. 4.28}$$

From now on, all the time scales will refer to the new time origin.

The next step is to solve $i_{1natural}$. We shall define a new symbol $i_{2input}(t_0)$ to represent $2\times i_2(t_0)$, so $i_{2input}(t_0) = 2I_{2max}\sin(\angle I_2 - \angle I_1)$. $i_{1natural}$ is produced by $i_{2input}(t_0)$. From Eq. 2.16, Chapter 2, we know that

$$\angle I_2 - \angle I_1 = Arc\tan(Q_2)$$

so there is

$$\sin(\angle I_2 - \angle I_1) = \frac{Q_2}{\sqrt{1+Q_2^2}}$$

Normally, $Q_2 >> 1$, so $\sin(\angle I_2 - \angle I_1) \approx 1$. Therefore, $i_2(t_0)$ in the following discussions will be approximately equal to $2I_{2max}$, that is

$$i_{2input}(t_0) \approx 2I_{2max}$$

4.6.3 The method for solving $i_{1natural}$

1) The Laplace transform of $i_{1natural}$

After t = t_0, the circuit configuration returns to normal like that in stage 1 (see Fig. 2.3 in Chapter 2). Using the same sign convention, the differential equation corresponding to the natural response is ($i_{1natural}$ and $I_{1natural}$ (s) is simplified as i_1 and I_1(s) in the equations):

$$\left.\begin{aligned} & R_1 i_1 + L_1 \frac{di_1}{dt} + \frac{1}{C_1}\int i_1 dt - M\frac{di_2}{dt} = 0 \\ & -M\frac{di_1}{dt} + L_2\frac{di_2}{dt} + \frac{1}{C_2}(\int i_2 dt - \int i_3 dt) = 0 \\ & \frac{1}{C_2}(\int i_3 dt - \int i_2 dt) + R_2 i_3 = 0 \end{aligned}\right\} \quad \text{------ Eq. 4.29}$$

Considering the initial condition $i_{2input}(t_0) \approx 2I_{2max}$, and performing the Laplace transform on Eq. 4.29 in the s domain (see Appendix 6 for Laplace transforms with initial conditions), results in

$$\left.\begin{aligned} & (R_1 + L_1 s + \frac{1}{C_1 s})I_1(s) - MsI_2(s) = -2M\,I_{2max} \\ & -M\,s\,I_1(s) + L_2\,s\,I_2(s) + \frac{1}{sC_2}\big(I_2(s) - I_3(s)\big) = 2L_2\,I_{2max} \\ & \frac{1}{sC_2}(I_3(s) - I_2(s)) + R_2 I_3(s) = 0 \end{aligned}\right\} \quad \text{------ Eq. 4.30}$$

The determinant of Eq. 4.30 is

$$\Delta(s)=\begin{vmatrix} R_1+L_1 s+\dfrac{1}{C_1 s} & -Ms & 0 \\ -Ms & L_2 s+\dfrac{1}{sC_2} & -\dfrac{1}{sC_2} \\ 0 & -\dfrac{1}{sC_2} & \dfrac{1}{sC_2}+R_2 \end{vmatrix}$$

and by Cramer's rule

$$I_1(s)=\frac{\Delta_1(s)}{\Delta(s)}=\frac{\begin{vmatrix} -2MI_{2\max} & -Ms & 0 \\ 2L_2 I_{2\max} & L_2 s+\dfrac{1}{sC_2} & -\dfrac{1}{sC_2} \\ 0 & -\dfrac{1}{sC_2} & \dfrac{1}{sC_2}+R_2 \end{vmatrix}}{\Delta(s)}$$

Expanding the above equation gives

$$I_1(s)=\frac{-\dfrac{2MR_2 I_{2\max}}{C_2 s}}{L_1 L_2 R_2 s^2-M^2 R_2 s^2+L_2 R_1 R_2 s+\dfrac{L_1 L_2 s}{C_2}-\dfrac{M^2 s}{C_2}+\dfrac{L_2 R_1}{C_2}+\dfrac{L_1 R_2}{C_2}+\dfrac{L_2 R_2}{C_1}+\dfrac{L_2}{C_1 C_2 s}+\dfrac{R_1 R_2}{C_2 s}+\dfrac{R_2}{C_1 C_2 s^2}}$$

Letting both nominator and denominator × s×C_2, gives

$$I_1(s)=\frac{-2MR_2 I_{2\max}}{C_2 L_1 L_2 R_2 s^3-C_2 M^2 R_2 s^3+C_2 L_2 R_1 R_2 s^2+L_1 L_2 s^2-M^2 s^2+L_2 R_1 s+L_1 R_2 s+\dfrac{C_2 L_2 R_2}{C_1}s+\dfrac{L_2}{C_1}+R_1 R_2+\dfrac{R_2}{C_1 s}}$$

Substituting M in the above equation by $M=k\sqrt{L_1 L_2}$ gives

$$I_1(s) = \frac{-2\,R_2\,k\sqrt{L_1 L_2}\,I_{2\max}}{C_2 L_1 L_2 R_2 s^3 - C_2 k^2 L_1 L_2 R_2 s^3 + C_2 L_2 R_1 R_2 s^2 + L_1 L_2 s^2 - k^2 L_1 L_2 s^2 + L_2 R_1 s + L_1 R_2 s + \frac{C_2 L_2 R_2}{C_1} s + \frac{L_2}{C_1} + R_1 R_2 + \frac{R_2}{C_1 s}}$$

From $\Omega = \frac{1}{\sqrt{L_1 C_1}} = \frac{1}{\sqrt{L_2 C_2}}$

we have $C_1 = \frac{1}{\Omega^2 L_1}$ *and* $L_2 = \frac{1}{\Omega^2 C_2}$

Letting them substitute C_1 and L_2 in the equation gives

$$I_1 = \frac{-2\,R_2\,k\sqrt{\frac{L_1}{\Omega^2 C_2}}\,I_{2\max}}{\frac{L_1 R_2}{\Omega^2} s^3 - \frac{k^2 L_1 R_2}{\Omega^2} s^3 + \frac{R_1 R_2}{\Omega^2} s^2 + \frac{L_1}{\Omega^2 C_2} s^2 - \frac{k^2 L_1}{\Omega^2 C_2} s^2 + \frac{R_1}{\Omega^2 C_2} s + 2L_1 R_2 s + \frac{L_1}{C_2} + R_1 R_2 + \frac{\Omega^2 L_1 R_2}{s}}$$

From $Q_1 = \frac{\Omega L_1}{R_1}$ and $Q_2 = R_2 C_2 \Omega$

we have

$R_1 = \frac{\Omega L_1}{Q_1}$ *and* $R_2 = \frac{Q_2}{C_2 \Omega}$

Bringing them into the equation gives

$$I_1(s) = \frac{-2\,\frac{Q_2}{C_2\Omega}\,k\sqrt{\frac{L_1}{\Omega^2 C_2}}\,I_{2\max}}{\frac{Q_2 L_1}{\Omega^3 C_2} s^3 - \frac{k^2 Q_2 L_1}{\Omega^3 C_2} s^3 + \frac{Q_2 L_1}{\Omega^2 Q_1 C_2} s^2 + \frac{L_1}{\Omega^2 C_2} s^2 - \frac{k^2 L_1}{\Omega^2 C_2} s^2 + \frac{L_1}{\Omega Q_1 C_2} s + 2L_1 \frac{Q_2}{C_2\Omega} s + \frac{L_1}{C_2} + \frac{Q_2 L_1}{Q_1 C_2} + \frac{\Omega Q_2 L_1}{s C_2}}$$

Letting both sides $\times \frac{\Omega^3 C_2}{Q_2 L_1}$ gives

$$I_1(s) = \frac{-2k\sqrt{\frac{1}{L_1 C_2}}\, s I_{2\max}}{s^4 - k^2 s^4 + \frac{\Omega}{Q_1}s^3 + \frac{\Omega}{Q_2}s^3 - \frac{\Omega k^2}{Q_2}s^3 + \frac{\Omega^2}{Q_1 Q_2}s^2 + 2\Omega^2 s^2 + \frac{\Omega^3}{Q_2}s + \frac{\Omega^3}{Q_1}s + \Omega^4}$$

Substituting L_1 with $L_1 = \frac{1}{\Omega^2 C_1}$, letting both sides $\times \frac{1}{1-k^2}$, rearranging each term in descending order by s and returning $I_1(s)$ to its actual name $I_{1natural}(s)$ give

$$I_{1natural}(s) = \frac{-\frac{2k\Omega^2}{1-k^2}\sqrt{\frac{C_1}{C_2}}\, s\, I_{2\max}}{s^4 + s^3\frac{\Omega\left(\frac{1}{Q_1}+\frac{1}{Q_2}-\frac{k^2}{Q_2}\right)}{1-k^2} + s^2\frac{\Omega^2\left(2+\frac{1}{Q_1 Q_2}\right)}{1-k^2} + s\frac{\Omega^3\left(\frac{1}{Q_1}+\frac{1}{Q_2}\right)}{1-k^2} + \frac{\Omega^4}{1-k^2}}$$

------ Eq. 4.31

2) Normalising $i_{1natural}$ and $I_{1natural}(s)$

Eq. 4.31 contains I_{2max}. In order to have $i_{1natural}$ compared with $i_{1steady}$ in Eq. 4.28, the primary current should be represented by I_{1max}. Comparing Eq. 2.11 and Eq. 2.15 gives:

$$\frac{I_{2\max}}{I_{1\max}} = \sqrt{\frac{C_2}{C_1}}\, k\sqrt{1+Q_2^2} \qquad \text{------ Eq. 4.32}$$

Substituting Eq. 4.32 into Eq. 4.31 yields

$$I_{1natural}(s) = \frac{-s\,\frac{2k^2\Omega^2}{1-k^2}\sqrt{1+Q_2^2}\;I_{1max}}{s^4 + s^3\frac{\Omega\left(\frac{1}{Q_1}+\frac{1}{Q_2}-\frac{k^2}{Q_2}\right)}{1-k^2} + s^2\frac{\Omega^2\left(2+\frac{1}{Q_1 Q_2}\right)}{1-k^2} + s\frac{\Omega^3\left(\frac{1}{Q_1}+\frac{1}{Q_2}\right)}{1-k^2} + \frac{\Omega^4}{1-k^2}}$$

------ Eq. 4.33[5]

It shows $I_{1natural}(s)$ is a function of k, Q_1, Q_2, Ω and I_{1max}.

3) The Inverse-Laplace transform to find the t-domain response of $i_{1natural}$

Eq. 4.33 is a ratio of polynomials in s, a rational function. One method of performing the inverse transformation of Eq. 4.33 is by definition $f(t)=\frac{1}{2\pi j}\int_{\alpha-j\infty}^{\alpha+j\infty}F(s)e^{st}\,ds$ and computing with the help of computer-aided software. However, symbolically computing with such complexity is beyond the capability of the available tools[6]. Alternatively, if typical component values are substituted for the symbols in Eq. 4.33, the software tools can calculate the inverse transformation numerically. But this will only yield a final result, which would not give a deeper insight into the fundamental relationships.

Other than attempting to calculate the Inverse-Laplace-Transformation directly, there is a general method [98], which decomposes Eq. 4.33 into a partial fraction expansion in the form

$$I_{1natural}(s) = \frac{r'}{s+\alpha'-j\omega'} + \frac{r'^*}{s+\alpha'+j\omega'} + \frac{r''}{s+\alpha''-j\omega''} + \frac{r''^*}{s+\alpha''+j\omega''} \qquad \text{------ Eq. 4.34}$$

The r', r'^*, r'' and r''^* are residues, $p'=-\alpha'+j\omega'$, $p'^*=-\alpha'-j\omega'$, $p''=-\alpha''+j\omega''$ and $p''^*=-\alpha''-j\omega''$ are poles. Not to lose generality, the residues and poles are assumed to be complex numbers, with real numbers being

[5] The result was re-derived and checked by the author's supervisor Tim Perkins.
[6] Matlab Symbolic toolbox and Mathematica have been tried.

regarded as special cases. Eq. 4.34 contains four terms: two of them have conjugate pairs of complex poles $-\alpha' \pm j\omega'$ and conjugate pairs of residues r', r'^*; the other two terms have conjugate pairs of complex poles $-\alpha'' \pm j\omega''$ and conjugate pairs of residues r'' and r''^*.

If the complex residues are written in polar form as

$$r' = |r'|e^{j\theta'}, r'^* = |r'|e^{-j\theta'} \text{ and } r'' = |r''|e^{j\theta''}, \; r''^* = |r''|e^{-j\theta''},$$

the Inverse-Laplace-transform of Eq. 4.34 is

$$i_{1natural} = 2|r'|e^{-\alpha' t}\cos(\omega' t + \theta') + 2|r''|e^{-\alpha'' t}\cos(\omega'' t + \theta'') \quad \text{------ Eq. 4.35}$$

Eq. 4.35 demonstrates that $i_{1natural}$ is the sum of two damped cosine waveforms. Each oscillates at radian frequency ω' or ω'' (called natural frequencies), but decays exponentially from peak value $|r'|$ or $|r''|$ to zero at a rate determined by damping time constant $1/\alpha'$ or $1/\alpha''$. The residues r' and r'' also determine the waveform's phases θ' and θ''.

So, if we could decompose Eq. 4.33 into the partial fraction expansion form of Eq. 4.34, the α', α'', ω', ω'', $|r'|$, $|r''|$, θ' and θ'' would be known, and the $i_{1natural}$ would subsequently be determined. However, in order to do so, the denominator in Eq. 4.33 has to be factorised into the form $(s+\alpha'+j\omega')(s+\alpha'-j\omega')(s+\alpha''+j\omega'')(s+\alpha''-j\omega'')$. This is difficult as it is a fourth order polynomial with complicated coefficients for each term. As has been discussed in the introduction to this chapter, one approach is to adopt Pierce's method to derive an analytical solution, which is presented in Appendix 7. The other is the author's approach, which numerically calculates α', α'', ω', ω'', $|r'|$, $|r''|$, θ' and θ'' with the aid of Matlab, analyses their behaviour, and derives the function of $i_{1natural}(t)$. This method is different from the direct Inverse-Laplace transform mentioned previously, as it relates the circuit parameters Q_1, Q_2 and k to α', α'', ω', ω'', $|r'|$, $|r''|$, θ' and θ'' instead of directly relating them to a final result. According to the

characteristics of α', α'', ω', ω'', $|r'|$, $|r''|$, θ' and θ'' along the k axis, the mathematical function can be made specific, helping gain insight into how the waveform is composed.

4) Partial fraction expansion using Matlab

This section explains the numerical partial-fraction expansion of rational function in Matlab. If we let vectors B and A specify the coefficients of the numerator and denominator polynomials in descending powers of s, the command

[r, p, D] = residue (B,A)

expands B(s)/A(s):

$$\frac{B(s)}{A(s)} = \frac{r(1)}{s-p(1)} + \frac{r(2)}{s-p(2)} + \text{-----} + \frac{r(n)}{s-p(n)} + D(s)$$

The residues are returned in the column vector r, the poles locate in column vector p, and the direct terms in vector D, which is empty if the length of vector B < length of vector A, as is the case in equation Eq. 4.33 [70].

If the circuit parameters (k, Q_1, Q_2, Ω and I_{1max}) are given, the coefficients of the numerator and denominator in Eq. 4.33 will be known. Therefore, r and θ', r'' and θ'' (residues and their angles), α' and α'' (the real part of the poles), ω' and ω'' (the imaginary part of the poles) can be calculated in Matlab by numerical partial-fraction expansion and analysed; $i_{1natural}$ can be constructed by Eq. 4.35. This approach will be adopted to analyse $i_{1natural}$ in the next chapter.

4.7 Summary

The modulation happens in three stages: the steady state, the switch-closure period and the period after the switch opens. The first two stages prepare for the conditions of modulation. In the last stage, the modulation is generated.

The hypothesis that closing the switch only for a short period has the effect of inverting the phase of $i_2(t)$ at $t = t_0$, but has no significant influence on the signals of the primary circuit is proved to be true only when k is small. However the study at

stage 2 shows the initial conditions for generating modulation can still be estimated based on this assumption, only it will result in a smaller response for higher *k*s. The initial conditions are summarised in Eq. 4.19, Eq. 4.20, Eq. 4.21, Eq. 4.22 and Eq. 4.17.

The modulation waveform generated after $t = t_0$ is a transient response. It is made up of a natural response superimposing onto the steady state response. Knowing the steady-state response, the problem is simplified by finding the natural response. Furthermore, by grouping the initial conditions in respect to the responses, the multi-inputs problem is simplified into a single input problem. The input is $i_{2input}(t_0) \approx 2I_{2max.}$

The mathematical expression of the natural response in the time domain can be derived by Laplace-transform and then Inverse Laplace-transform by partial fraction expansion to obtain Eq. 4.35. But it is difficult because the denominator in Eq. 4.33 is a fourth order polynomial with complicated coefficients for each term. A method which numerically executes partial-fraction expansion in Matlab and analyses the behaviours of α', α'', ω', ω'', $|r'|$, $|r''|$, θ' and θ'' along the k axis to derive the function of $i_{1natural}(t)$ will be used in the next chapter.

Chapter 5 Analysis of Passive Phase Shift Modulation – Part 2

5.1 Introduction

This chapter will study the circuit response i_l (or $i_{l\text{transient}}$) after $t = t_0$ (stage 3). As has been discussed in Chapter 4, i_l ($t > t_0$) consists of both a steady-state response and a natural response. Hence, the investigation will consider each response separately, and sum them later. Rewriting Eq. 4.26 of Chapter 4 here

$$i_{l\text{transient}} = i_{l\text{steady}} + i_{l\text{natural}} \qquad \text{------Eq. 5.1}$$

The steady-state response $i_{l\text{steady}}$ was found in Chapter 2. The natural response $i_{l\text{natural}}$ will be studied in this chapter. It is conducted by substituting the parameters in Eq. 4.33 of Chapter 4 with numerical data, executing partial fraction expansion in Matlab to give $|r'|$, $|r''|$, θ', θ'', α', α'', ω' and ω'', and observing their relations along the k axis to derive the function of $i_{l\text{natural}}$. For convenient reference, Eq. 4.28, Eq. 4.33, Eq. 4.35 from Chapter 4 are rewritten here:

$$i_{1steady}(t) = -I_{1\max}\sin(\Omega t) \qquad \text{------Eq. 5.2}$$

$$I_{lnatural}(s) = \frac{-s\,\frac{2k^2\Omega^2}{1-k^2}\sqrt{1+Q_2^2}\;I_{1\max}}{s^4 + s^3\frac{\Omega\left(\frac{1}{Q_1}+\frac{1}{Q_2}-\frac{k^2}{Q_2}\right)}{1-k^2} + s^2\frac{\Omega^2\left(2+\frac{1}{Q_1Q_2}\right)}{1-k^2} + s\frac{\Omega^3\left(\frac{1}{Q_1}+\frac{1}{Q_2}\right)}{1-k^2} + \frac{\Omega^4}{1-k^2}} \qquad \text{------Eq. 5.3}$$

$$i_{1natural} = 2|r'|e^{-\alpha' t}\cos(\omega' t + \theta') + 2|r''|e^{-\alpha'' t}\cos(\omega'' t + \theta'') \qquad \text{-------Eq. 5.4}$$

The amplitude, the waveform shape and the duration of i_1 ($t > t_0$) will then be discussed. So will the influence of Q_1 or Q_2 on the modulation. The k working range will be evaluated.

5.2 Response of $i_{1natural}$

5.2.1 Introduction

All diagrams and locus curves in this section are calculated using the optimal parameters obtained in Chapter 2 (unless stated otherwise), and let I_{1max} be unity. They are:

$$\left.\begin{array}{l} Q_1 = 53 \\ Q_2 = 12 \\ f_0 = 4\ \text{MHz} \\ \Omega = 2\pi f_0 \\ I_{1max} = 1 \\ 0.01 \le k \le 0.16 \end{array}\right\} \quad \text{------Eq. 5.5}$$

Sample k between $0.01 \le k \le 0.16$, substitute Eq. 5.5 into Eq. 5.3, and calculate the poles and residues in Matlab for each k. From the real part of the poles α' and α'', we have the corresponding time constant $1/\alpha'$ and $1/\alpha''$; from the imaginary parts ω' and ω'', we have the corresponding damped frequency $f_d' = \omega'/2\pi$ and $f_d'' = \omega''/2\pi$; we also have the absolute values of residues $|r'|$ and $|r''|$, and the angles of the residues θ' and θ''. Plot $1/\alpha'$ and $1/\alpha''$ versus k in Fig. 5.1 A; f_d' and f_d'' versus k in Fig. 5.1 B; $|r'|$ and $|r''|$ versus k in Fig. 5.1 C; and θ' and θ'' versus k in Fig. 5.1 D.

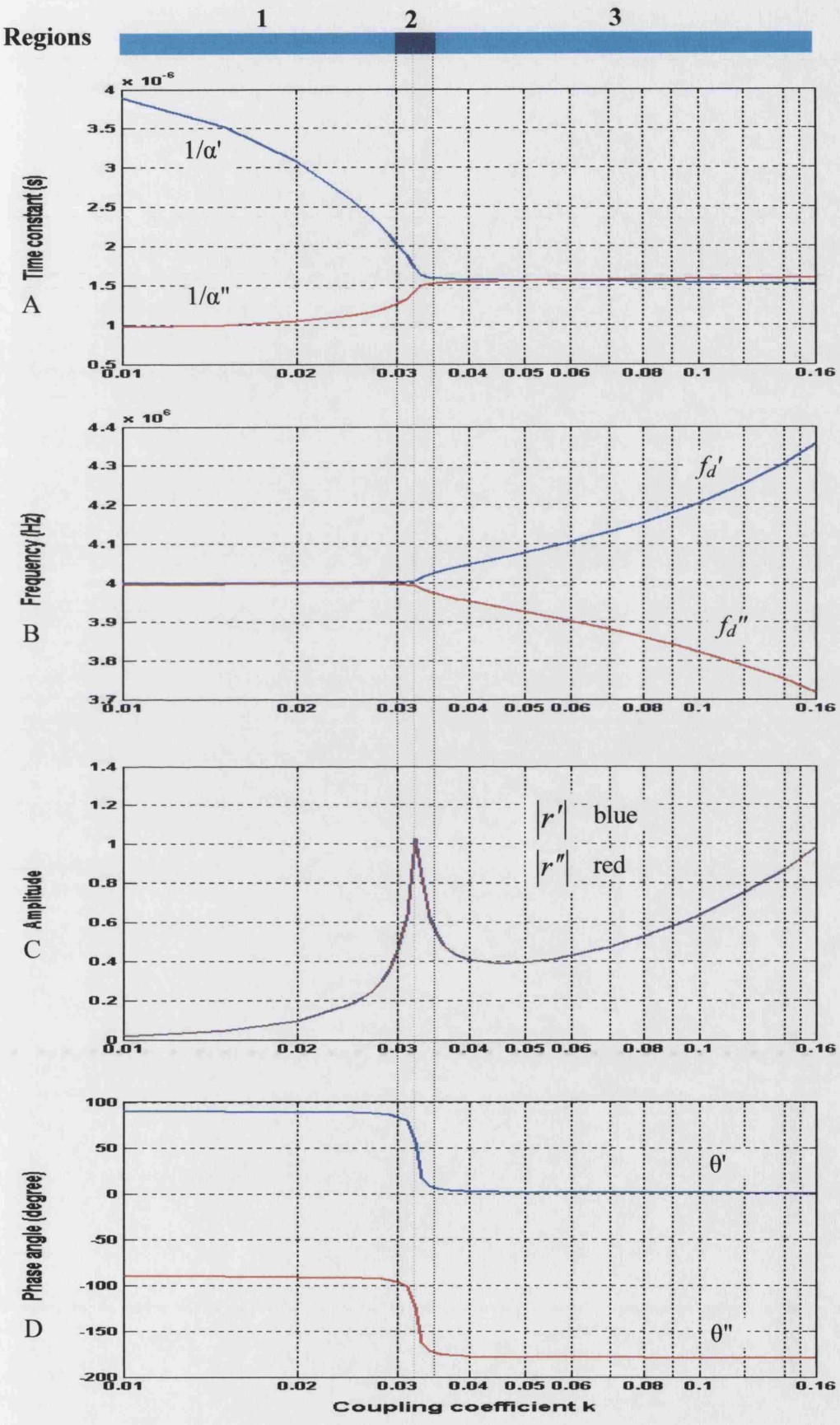


Fig. 5.1 1/α', 1/α", f_d', f_d'', $|r'|$, $|r''|$, θ' and θ" versus k.

Fig. 5.1 demonstrates how the behaviour of $1/\alpha'$, $1/\alpha''$, ω', ω'', $|r'|$, $|r''|$, θ' and θ'' change when the secondary circuit approaches the primary circuit (indicated by the increasing k value). The blue curves in each figure represent parameters for the first damped cosine in Eq.4.35, the red one is for the second damped cosine.

These parameters have distinguishing features in three k regions, which are marked on the top of the figure:

Region 1: $k < 0.03$

Region 2: $0.03 \leq k < 0.034$

Region 3: $0.034 \leq k < 0.16$

However, it should be borne in mind that the boundaries between the regions are not clear-cut. The next step is to analyse each region in detail. Note that the common feature of all the regions is $|r'| \approx |r''| \approx |r|$.

5.2.2 Origin where $k \approx 0$

When the primary and secondary circuits are far apart, where $k \approx 0$, $1/\alpha'$ and f_d' are actually the time constant and damped frequency of the primary circuit $1/\alpha_1$ and f_{d1}; $1/\alpha''$ and f_d'' are the time constant and damped frequency of the secondary circuit, $1/\alpha_2$, and f_{d2}; that is

$$1/\alpha' \approx 1/\alpha_1 = 2Q_1/\Omega, \text{ and } f_d' \approx f_{d1} = \frac{1}{2\pi}\sqrt{\Omega^2 - (\frac{\Omega}{2Q_1})^2}$$

$$1/\alpha'' \approx 1/\alpha_2 = 2Q_2/\Omega, \text{ and } f_d'' \approx f_{d2} = \frac{1}{2\pi}\sqrt{\Omega^2 - (\frac{\Omega}{2Q_2})^2}$$

This can be verified by substituting Eq. 5.5 into the above equations. It gives $1/\alpha_1 \approx 4.2\times10^{-6}$ s, $f_{d1} \approx 4$ MHz and $1/\alpha_2 \approx 0.96\times10^{-6}$ s, $f_{d2} \approx 4$ MHz. By extending the k axis in Fig. 5.1 A and B to the left, the blue and red curves will approach these values respectively.

5.2.3 Region 1 ($k < 0.03$)

In this region, the two circuits gradually affect each other. $1/\alpha'$ and f_d' are no longer the attributes of the primary circuit alone, and $1/\alpha''$ and f_d'' are no longer the attributes of the secondary circuit alone; they coexist in both circuits. As the time constants $1/\alpha'$ and $1/\alpha''$ are more heavily influenced by the opposite circuit, the blue and red curves in Fig. 5.1 A are drawn towards an intermediate value. But the difference between $1/\alpha'$ (blue) and $1/\alpha''$ (red) is still large. There is

$$1/\alpha' > 1/\alpha'' \qquad \text{------Eq. 5.6}$$

and

$$f_d' \approx f_d'' \approx f_0$$

$$|r'| \approx |r''| \approx |r| \qquad \text{------Eq. 5.7}$$

$$\theta' \approx \pi/2,\ \theta'' \approx -\pi/2$$

Substituting them into Eq. 5.4, gives

$$i_{1natural}(t) \approx 2|r'|e^{-\alpha' t}\cos(\Omega t + \frac{\pi}{2}) + 2|r''|e^{-\alpha'' t}\cos(\Omega t - \frac{\pi}{2})$$

$$\approx 2\left(e^{-\alpha' t} - e^{-\alpha'' t}\right)|r|\ (-\sin(\Omega t)) \qquad \text{------Eq. 5.8}$$

Eq. 5.8 shows that the compound waveform oscillates at the resonant frequency, with the envelope being determined by the difference of the two exponentials. Fig. 5.2 illustrates two individual waveforms in blue and red, and the sum of the two (equivalent to Eq. 5.8) in green. Note that the amplitude of the summed waveform is smaller than that in each individual waveform, and the duration of $i_{1natural}$ is determined by the longer time constant (the blue curve).

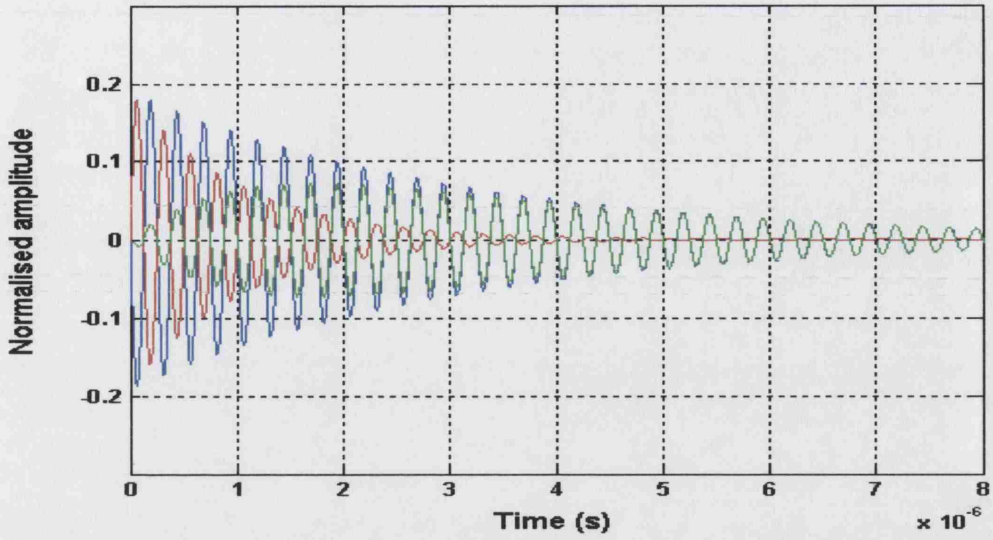


Fig. 5.2 $i_{1natural}$ in region 1 (plotted for k = 0.02).

5.2.4 Region 3 ($0.034 \leq k < 0.16$)

Region 2 will be discussed after this section. In region 3, $1/\alpha'$ and $1/\alpha''$ are approximately equal; f_d' and f_d'' split; θ' approaches to 0 and θ'' to $-\pi$. To summarise,

$$\left.\begin{array}{l} 1/\alpha' \approx 1/\alpha'' \approx 1/\alpha \\ f_d' > f_d'' \\ |r'| \approx |r''| \approx |r| \\ \theta' \approx 0,\ \theta'' \approx -\pi \end{array}\right\} \quad \text{------Eq. 5.9}$$

Substituting them into Eq. 5.4, gives

$$i_{1natural}(t) \approx 2|r|e^{-\alpha t}\cos(\omega' t)+2|r|e^{-\alpha t}\cos(\omega'' t-\pi)$$

$$=-4|r|\,e^{-\alpha t}\,\sin(\frac{\omega'-\omega''}{2}t)\sin(\frac{\omega'+\omega''}{2}t)$$

$$=4|r|\,e^{-\alpha t}\,\sin(\frac{\omega'-\omega''}{2}t)\;(-\sin(\frac{\omega'+\omega''}{2}t)) \qquad \text{------ Eq. 5.10}$$

This is a product of an exponential function and two sine functions. What is the waveform shape?

By definition, the exponential waveform $e^{-\alpha t}$ has a duration lasting approximately five times $1/\alpha$, denoted as

$$T_e = 5/\alpha \qquad \text{------ Eq. 5.11}$$

The first sine function in Eq. 5.10 has a period of

$$T_{sine1}=\frac{4\pi}{\omega'-\omega''} \qquad \text{------ Eq. 5.12}$$

While the second sine function has a period of

$$T_{sine2}=\frac{4\pi}{\omega'+\omega''} \qquad \text{------ Eq. 5.13}$$

From Fig. 5.1 B, we see $f_d' - f_d''$ is much less than the individual f_d' (or f_d''), denoted as $(f_d' - f_d'') \ll f_d'$ (or f_d''). Therefore, there is $T_{sine1} \gg T_{sine2}$. So $i_{1natural}(t)$'s envelope shape depends on the relation between T_e and T_{sine1}, resulting in two types of shape: when T_e is comparable or less than T_{sine1}, the composite waveform will look like the red curve in Fig. 5.3. It has one obvious peak; in Fig. 5.4, when $T_e \gg T_{sine1}$, the composite waveform will beat at a frequency of $2/T_{sine1}$, and the peaks of the beats decline exponentially.

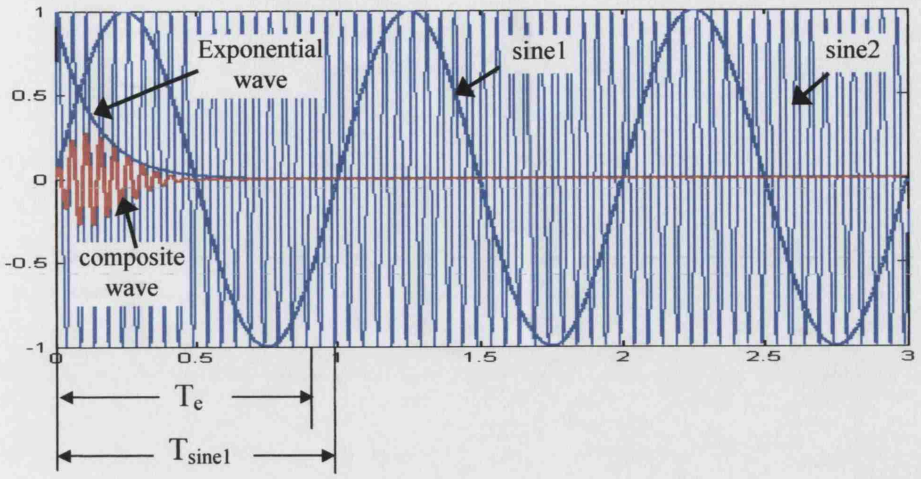


Fig. 5.3 One of the waveform types in region 3 when $T_e \leq T_{sine1}$.

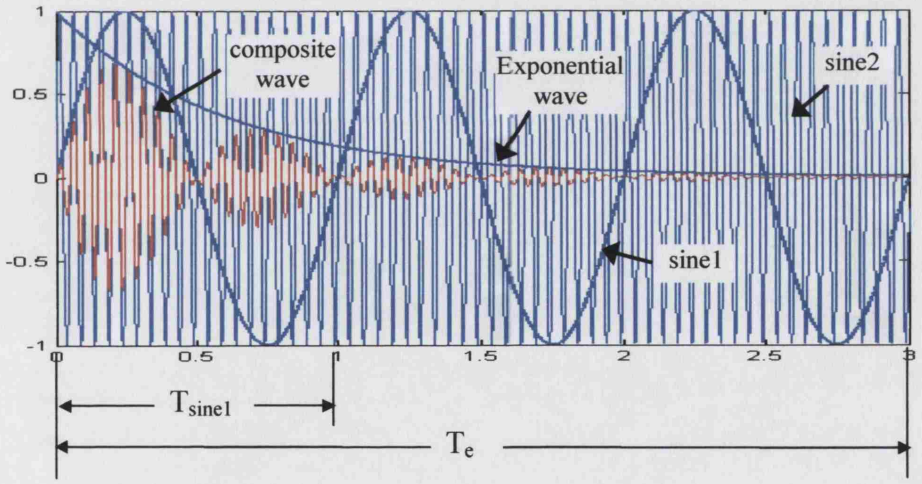


Fig. 5.4 Another waveform type in region 3 when $T_e >> T_{sine1}$.

Which type of waveform is likely to occur? This can be examined by comparing T_e and T_{sine1}. T_e and T_{sine1} are calculated from Eq. 5.11 and Eq. 5.12, and illustrated in Fig. 5.5, in which α_1 is used to represent α in Eq. 5.11. The figure shows that when $k \leq 0.07$, then $T_e \leq T_{sine1}$, thus $i_{1natural}(t)$ will show one large peak; and when $k > 0.07$, $T_e > T_{sine1}$, so $i_{1natural}(t)$ will have more beats. For example, T_e/T_{sine1} is about 2.4 at $k = 0.16$, and 5 beats are expected to appear in $i_{1natural}(t)$.

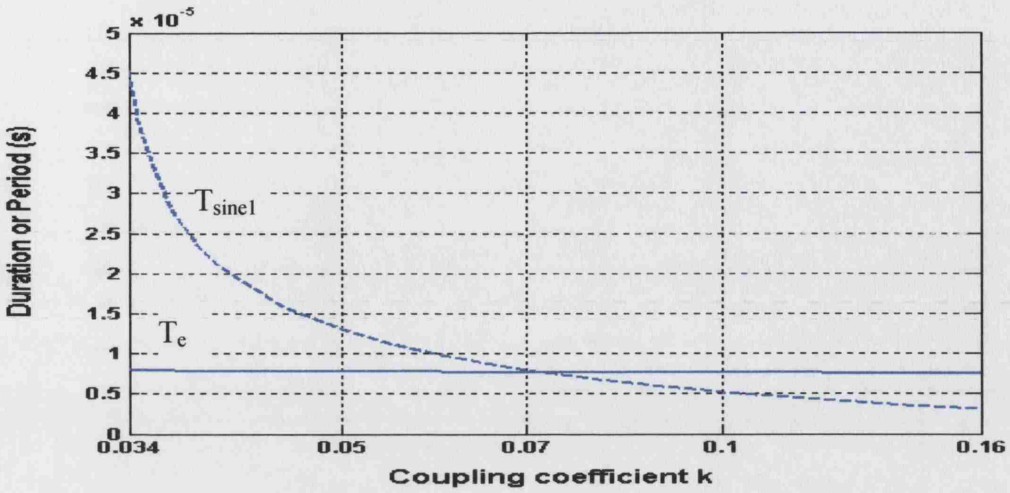


Fig. 5.5 Comparison of T_e and T_{sine1}

Fig. 5.6 plots $i_{1natural}(t)$ in time domain by Eq. 5.10. It shows there is a single peak at $k = 0.05$, and five beats at $k = 0.16$. They agree with the prediction.

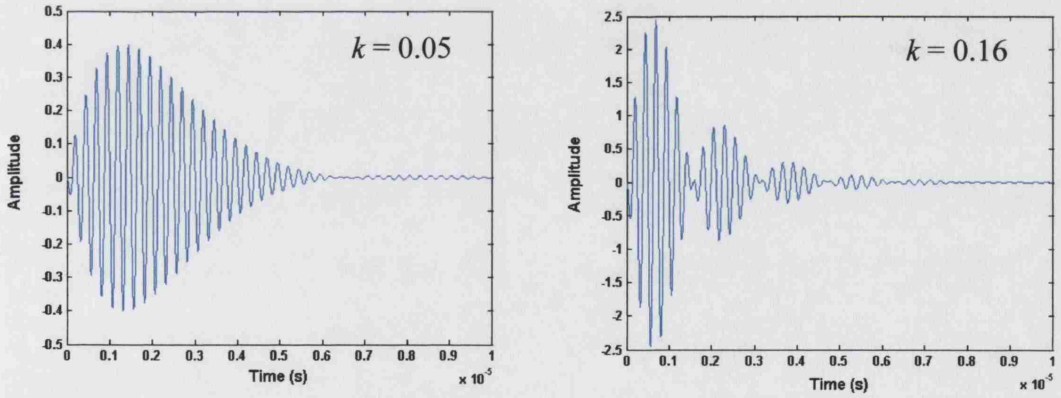


Fig. 5.6 $i_{1natural}(t)$ at $k = 0.05$ and $k = 0.16$

5.2.5 Region 2 ($0.03 \le k < 0.034$)

In this region, $|r'|$ and $|r''|$ increase to a high level then drop back; θ' is decreases from $\pi/2$ to 0, and θ'' is decreases from $-\pi/2$ to $-\pi$; $1/\alpha'$ and $1/\alpha''$ begin to approach each other; and f_d' and f_d'' start to split.

The relations are

$$\left.\begin{aligned} &1/\alpha' > 1/\alpha'' \\ &f_d' > f_d'' \\ &|r'| \approx |r''| \approx |r| \end{aligned}\right\} \quad \text{------ Eq. 5.14}$$

Also there are

$$\left.\begin{aligned} &\theta'-\theta'' = \pi \\ &\theta' + \theta'' = \theta,\ (-\pi < \theta < 0) \end{aligned}\right\} \quad \text{------ Eq. 5.15}$$

So that,

$$\left.\begin{aligned} &\theta' = \frac{\pi}{2} + \frac{\theta}{2} \\ &\theta'' = \frac{\theta}{2} - \frac{\pi}{2} \end{aligned}\right\} \quad \text{------ Eq. 5.16}$$

By Eq. 5.14 and Eq. 5.4, we shall have

$$i_{1natural}(t) \approx 2|r|e^{-\alpha' t}\cos(\omega' t + \theta') + 2|r|e^{-\alpha'' t}\cos(\omega'' t + \theta'') \quad \text{------ Eq. 5.17}$$

By Eq. 5.16 and Eq. 5.17, we shall have

$$i_{1natural}(t) \approx 2|r|e^{-\alpha' t}\cos(\omega' t + \frac{\theta}{2} + \frac{\pi}{2}) + 2|r|e^{-\alpha'' t}\cos(\omega'' t + \frac{\theta}{2} - \frac{\pi}{2})$$

$$\approx -2|r|\left(e^{-\alpha' t}\sin(\omega' t + \frac{\theta}{2}) - e^{-\alpha'' t}\sin(\omega'' t + \frac{\theta}{2})\right) \quad \text{------ Eq. 5.18}$$

Expanding Eq. 5.18 and grouping, gives

$$i_{1natural}(t)$$
$$\approx -2|r|\cos(\frac{\theta}{2})\left(e^{-\alpha' t}\sin(\omega' t)-e^{-\alpha'' t}\sin(\omega'' t)\right)+2|r|\left(-\sin(\frac{\theta}{2})\right)\left(e^{-\alpha' t}\cos(\omega' t)-e^{-\alpha'' t}\cos(\omega'' t)\right)$$

Part 1 Part 2

-------Eq. 5.19

Eq. 5.19 shows that $i_{1natural}(t)$ in this region is made of two parts. Part 1 has a coefficient $\cos(\frac{\theta}{2})$, and part 2 has a coefficient $(-\sin(\frac{\theta}{2}))$. $\theta/2$ in Eq. 5.19 is the average of θ' and θ'', and its value drops from approximately 0 to approximately $-\pi/2$ across the region. This means the amount of contribution from the part 1 is dropping from near 100% to 0% because $\cos(\frac{\theta}{2})$ drops from 1 to 0; and that from part 2 increases from 0% to 100% because $(-\sin(\frac{\theta}{2}))$ is from 0 increasing to 1. The middle point where part 1 and part 2 contribute equally is where the peaks of $|r'|$ and $|r''|$ are.

If we assume that at the beginning of region 2, f_d' is still regarded as approximately equal to f_d'', which is $f_d' \approx f_d'' \approx f_0$, with $\cos(\frac{\theta}{2}) \approx 1$ and $\sin(\frac{\theta}{2}) \approx 0$, Eq. 5.19 would include part 1 only and become

$$i_{1natural} \approx part1 \approx 2|r|(e^{-\alpha' t} - e^{-\alpha'' t})(-\sin(\Omega t))$$

It is the same as Eq. 5.8 which represents the waveform in region 1.

If we assume that at the end of region 2, α_1 is regarded as approximately equal to α_2, which is $1/\alpha' \approx 1/\alpha'' \approx 1/\alpha$, with $\cos(\frac{\theta}{2}) \approx 0$ and $\sin(\frac{\theta}{2}) \approx -1$, Eq. 5.19 would include part 2 only and become

$$i_{1natural} \approx part2 \approx 4|r|\, e^{-\alpha t}\, \sin(\frac{\omega' - \omega''}{2} t)\ \ (-\sin(\frac{\omega' + \omega''}{2} t))$$

It is the same as Eq. 5.10, which represents the waveform in region 3.

So, region 2 is a buffer region between region 1 and region 3. In Fig. 5.7 $i_{1natural}$ is plotted by Eq. 5.19 at the beginning, middle and end of region 2. Close examination finds that the waveform shapes are identical and the high frequency components within the envelopes are minus-sine functions at 4 MHz. The envelope amplitude gradually increases across the region. The rapid peaking of $|r'|$ and $|r''|$ shown in Fig. 5.1 C is unnoticeable in the compound waveforms because large $|r'|$ and $|r''|$ is compensated by the small differences between $1/\alpha'$ and $1/\alpha''$, and also between f_d' and f_d''.

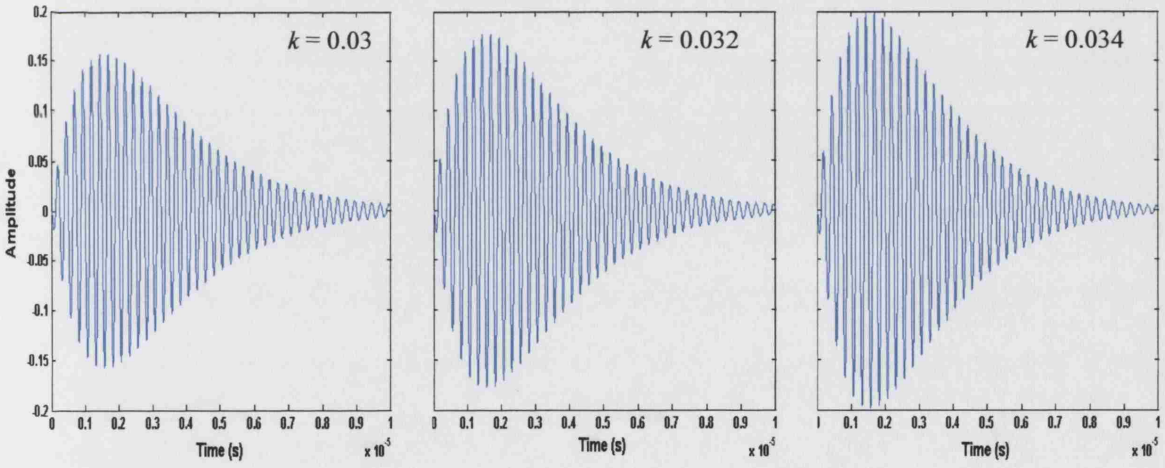


Fig. 5.7 $i_{natural}$ in region 2.

5.2.6 Amplitude of $i_{1natural}$

Although Fig. 5.1 C gives $|r'|$ and $|r''|$, which are amplitudes of the two individual damped cosines in Eq.5.4, the maximal amplitude of the compound waveform $i_{1natural}$ is not obvious by directly judging the formulae. We only know that at very weak

coupling (region 1) it is in the form of $2\left(e^{-\alpha' t}-e^{-\alpha'' t}\right)|r|$, and when k gets larger (region 3), it is in the form $4|r|\, e^{-\alpha t}\, \sin(\frac{\omega'-\omega''}{2})$.

It is easier to examine it numerically. If the circuit parameters are given, $1/\alpha'$, $1/\alpha''$, f_d', f_d'', $|r'|$, $|r''|$, θ' and θ'' can be calculated as before; $i_{1natural}$ can be constructed by Eq. 5.4; and its maximal amplitude can be found in Matlab. Fig. 5.8 plots the amplitude versus k using the parameters from Eq. 5.5. It shows that the amplitude varies from 0.019 at $k = 0.01$ to 2.5 at $k = 0.16$. The increase rate is rapid.

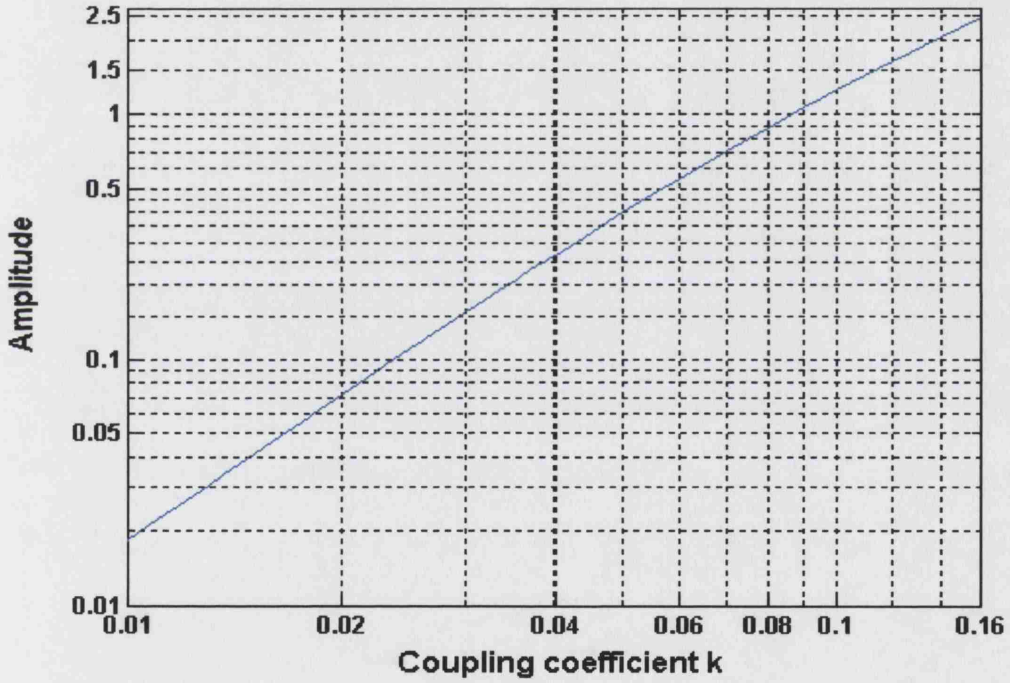


Fig. 5.8 The maximal amplitude of $i_{1natural}$ versus k (Q_1 = 53, Q_2 = 12).

5.3 Complete circuit response $i_{1transient}$

5.3.1 Formulae

The complete circuit response is obtained by Eq. 5.1, which is the sum of $i_{1steady}$ and $i_{1natural}$. As $I_{1max} = 1$, the final form of the function is:

In region 1, Eq. 5.2 plus Eq. 5.8

$$i_{1transient} \approx -\sin(\Omega t) + 2\left(e^{-\alpha' t} - e^{-\alpha'' t}\right)|r|\ (-\sin(\Omega t))$$

$$= (1 + 2\left(e^{-\alpha' t} - e^{-\alpha'' t}\right)|r|)\ (-\sin(\Omega t)) \qquad \text{------ Eq. 5.20}$$

In region 2, Eq. 5.2 plus Eq. 5.19

$$i_{1natural}(t) \approx -\sin(\Omega t)$$
$$-2|r|\cos(\frac{\theta}{2})\left(e^{-\alpha' t}\sin(\omega' t) - e^{-\alpha'' t}\sin(\omega'' t)\right) + 2|r|\left(-\sin(\frac{\theta}{2})\right)\left(e^{-\alpha' t}\cos(\omega' t) - e^{-\alpha'' t}\cos(\omega'' t)\right)$$

------ Eq. 5.21

In region 3, Eq. 5.2 plus Eq. 5.10

$$i_{1transient} \approx -\sin(\Omega t) + 4|r|\, e^{-\alpha t}\ \sin(\frac{\omega' - \omega''}{2} t)\ (-\sin(\frac{\omega' + \omega''}{2} t)) \qquad \text{------ Eq. 5.22}$$

In most parts of region 3, the average frequency $\frac{f_d' + f_d''}{2}$ is near f_0, or $\Omega \approx \frac{\omega' + \omega''}{2}$. For example, Fig. 5.9 shows the plot of $\frac{f_d' + f_d''}{2}$, which is calculated from Fig. 5.1 B, and the plot of f_0 = 4 MHz. Comparing them, the difference is less than 1% ($=\frac{4.04 - 4}{4}$) at k = 0.16. Therefore, because $\Omega \approx \frac{\omega' + \omega''}{2}$ in region 3, Eq. 5.22 is simplified as

$$i_{1transient} \approx (1 + 4|r|\, e^{-\alpha t}\ \sin(\frac{\omega' - \omega''}{2} t))\ (-\sin(\Omega t)) \qquad \text{------ Eq. 5.23}$$

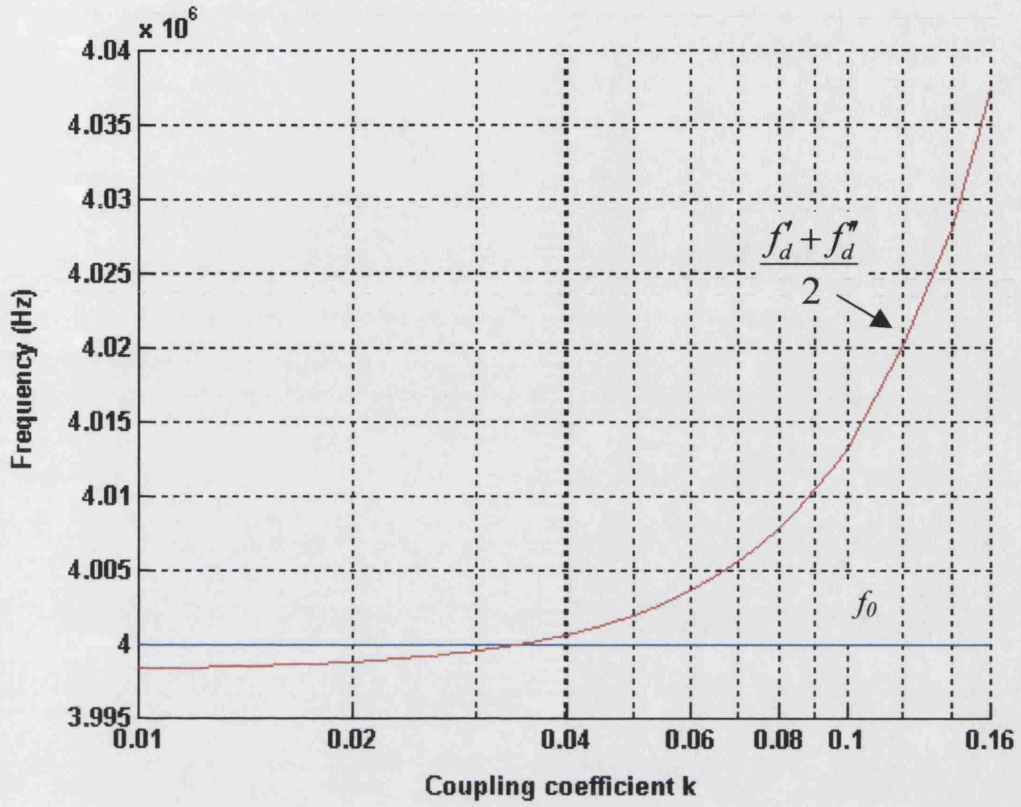


Fig. 5.9 Comparison of f_0 to $\frac{f_d' + f_d''}{2}$

5.3.2 Amplitude

In region 1, 2 and 3, $i_{1steady}$ and $i_{1natural}$ are both a minus sine function if the envelope shapes are disregarded. So the amplitude of $i_{1transient}$ is the amplitude of $i_{1natural}$ plus 1, where 1 is the amplitude of the $i_{1steady}$.

Sometimes, when Q_1, Q_2 and k have other values, $\frac{\omega' + \omega''}{2}$ might not be regarded as equal to Ω. $i_{1steady}$ and $i_{1natural}$ will have different frequencies and phases. $i_{1transient}$ is then composed in a more complicated way. However, this situation, if it happens, is often at the upper end of region 3 where the amplitude of $i_{1natural}$ is rather large and a dominant factor in $i_{1transient}$. Therefore, the influence of $i_{1steady}$ is relatively small, so the influence of the frequency difference is small. As an approximation, the amplitude of $i_{1transient}$ can still be $i_{1natural}$ plus 1.

5.3.3 Waveform shape

When $i_{1natural}$ has only one peak, which is the case in region 1, 2 and part of region 3 ($k < 0.07$), it simply adds to $i_{1steady}$ so that $i_{1transient}$ has the same waveform shape as $i_{1natural}$, but the amplitude is increased by 1. See Fig. 5.10 A.

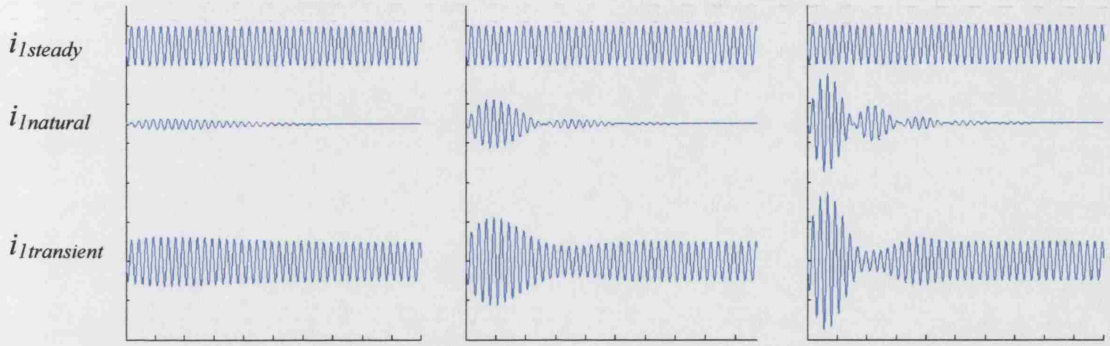


Fig. 5.10 $i_{1steady}$, $i_{1natural}$ *and compound* $i_{1transient}$. *All amplitudes are normalised to* I_{1max}.

When $i_{1natural}$ has more than two beats, the shape of $i_{1transient}$ is different from $i_{1natural}$ because, if counting the beats along the time axis, the odd beats (1st, 3rd etc.) add to $i_{1steady}$, while the even beats (2nd, 4th, etc.) subtract from $i_{1steady}$. The situation of Fig. 5.10 B and C results in only one obvious beat in the $i_{1transient}$. This means $i_{1steady}$ helps to reduce the beat phenomenon. However, as the $i_{1natural}$ beats more often when k gets greater, its amplitude also becomes greater than that of $i_{1steady}$. $i_{1natural}$ becomes the dominant component in the $i_{1transient}$, making $i_{1steady}$ less effective in smoothing the beats.

5.3.4 Waveform duration

The duration of $i_{1natural}$ is the duration of $i_{1transient}$. It is determined by one of the damped cosine waveforms, the one which has a longer time constant in Eq. 5.4. In region 1 and 2, the longer time constant is $1/\alpha'$; in region 3, $1/\alpha'$ approximately equals $1/\alpha''$. Hence, for all the regions, we let

The waveform duration $\approx 5 \times 1/\alpha'$ ------ Eq. 5.24

5.3.5 Verifying the analytical result

Eq. 5.20, Eq. 5.21, Eq. 5.22 and Eq. 5.23 are derived according to the features of $1/\alpha'$, $1/\alpha''$, f_d', f_d'', $|r'|$, $|r''|$, θ' and θ'' along the k axis. Some of the approximation have been made to simplify the mathematical expressions. In this section, these expressions will be verified by simulation in OrCAD PSpice.

The simulation circuit is shown in Fig. 5.11. The component values are given by Table 2.3, Chapter 2, and are equivalent to Eq. 5.5 if represented by Q_1 and Q_2.

The procedure is: in OrCAD, run simulations at a number of ks in region 1, 2 and 3, record the primary current i_1; in Matlab, calculate $i_{1transient}$ at the same k by Eq. 5.20, Eq. 5.21, Eq. 5.22 or Eq. 5.23 depending on the regions, and plot $i_{1transient}$ versus *time*; then compare the two sets of result. Fig. 5.12 shows three of the comparisons at k = 0.03, 0.1 and 0.16. Fig. 5.12 A, C and E are the measurements from the simulations; they are normalised by the corresponding primary current amplitude in the steady-state. Fig. 5.12 B, D and F are from the calculations.

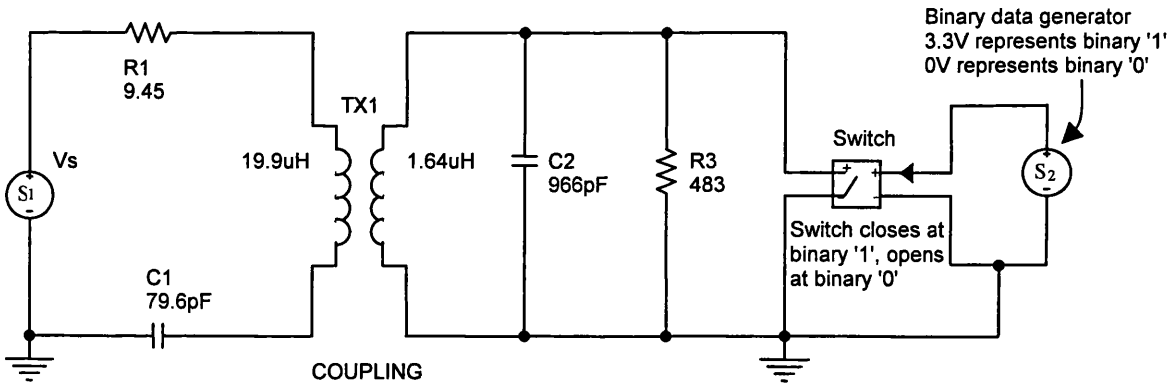


Fig. 5.11 The circuit used in the simulation for verifying the analytical results.

Fig. 5.12 shows that the calculated waveforms agree with the simulated waveform. It indicates that the approximations when deriving the formulae are justified.

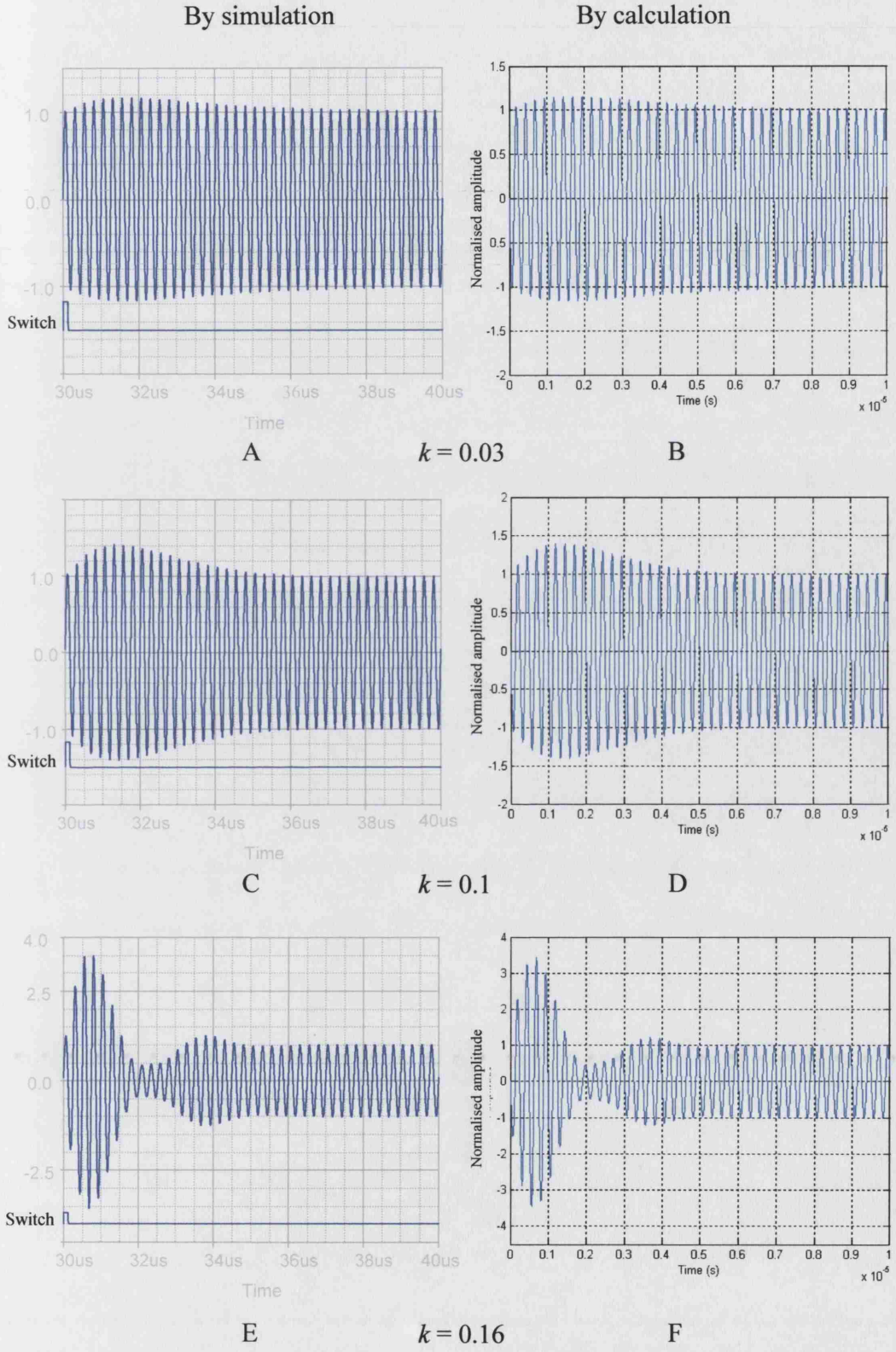


Fig. 5.12 Comparing the simulation results and calculated results of $i_{1transient}(t)$.

5.3.6 Summary of the circuit response of $i_1(t)$ ($t > t_0$)

$i_1(t)$ briefly increases after $t = t_0$. This transient response is denoted as $i_{transient}$ in this section. It is made by the natural response $i_{natural}$ superimposing onto the steady-state response i_{steady}. The natural response $i_{natural}$ is itself a compound waveform comprising two damping cosine functions (Eq. 5.4). Depending on the properties of $1/\alpha'$, $1/\alpha''$, f_d', f_d'', $|r'|$, $|r''|$, θ' and θ'' along the k axis, $i_{natural}$ can be expressed by Eq. 5.8, Eq. 5.19 and Eq. 5.10. Despite the differences in these equations, $i_{natural}$ is an approximate minus sine function (-sin(Ωt)) under the various envelop shapes. The steady-state i_{steady}, is also a minus sine function (-sin(Ωt)). So adding $i_{natural}$ to i_{steady}, makes $i_{transient}$ increase. The transient response has a single peak at the lower k, and shows a beat phenomenon at the larger k. The duration of the transient response is determined by the time constant $1/\alpha'$ (Eq. 5.24). The modulation amplitude is small for the weak coupling, but very large when k is greater.

5.4 Criteria for evaluating the k working range

The above analysis shows that, within a range of k, the transient response is large enough to be detectable and has a good waveform shape to represent a modulation. How to determine this k range?

Detectability is indicated by the modulation index. If A be the maximal amplitude of $i_{transient}$, and B be the amplitude of i_{steady}, the modulation index m is

$$m = \frac{A - B}{A + B}$$

We know A = the maximal amplitude of $i_{1natural} + 1$, B = 1, so

$$m = \frac{the\ \max\ amplitude\ of\ i_{1natural}}{the\ \max\ amplitude\ of\ i_{1natural} + 2} \qquad \text{------ Eq. 5.25}$$

If the minimal detectable m is provisionally set as 0.01, the lower boundary of k where the *PPSM* works can be estimated. In our example, calculated from Eq. 5.25 and Fig. 5.8, we know that at $k = 0.01$, $m \approx 0.01$. So $k \geq 0.01$ is the minimal working value.

A beating waveform is not suitable for indicating a modulation because it might be falsely taken as several modulations instead of a single one. Therefore, there is an upper limit of k, beyond which the waveform shape beats too much, and thus is unsuitable for representing a modulation. However, this limit or boundary is rather flexible, depending on the ability of the demodulation circuit. If we take $i_{1transient}$ in Fig. 5.10 C as an acceptable waveform just within the boundary, the condition for it to occur is that the corresponding $i_{1natural}$ has less than five beats. From the previous discussion on Fig. 5.5 and Fig. 5.6, we know that the condition for such an $i_{1natural}$ to occur is $T_e/T_{sine1} \leq 2.5$. Therefore, in this thesis, the condition which limits the upper boundary of the k is defined as $T_e/T_{sine1} \leq 2.5$.

To summarise, the lower k boundary is where $m \geq 0.01$ is true and the upper k boundary is where $T_e/T_{sine1} \leq 2.5$ is true. These criteria will be cited in the following sections when discussing the influence of Q_1 and Q_2 on the working range.

5.5 Influence of Q_1, Q_2 on PPSM

5.5.1 Introduction

Eq. 5.3 shows the modulation is the function of k, Q_1, Q_2, Ω, I_{1max}. But because Ω, I_{1max} can be normalised, the real variables are k, Q_1, Q_2. We have analysed how the modulation waveform develops along the k axis when Q_1 and Q_2 are given and have concluded PPSM works within a certain range of the k. But when the k is either too large or too small, the modulation waveform does not have a good shape.

The following sections will discuss the influence of Q_1, Q_2 on PPSM and will assess the k working range when Q_1, Q_2 are at different values. Firstly, we will examine the changes of $1/\alpha'$, $1/\alpha''$, f_d', f_d'', $|r'|$, $|r''|$, θ' and θ'' when Q_1 or Q_2 varies. From those parameters, the modulation index m and T_e/T_{sine1} ratio will then be derived; hence, the working conditions $m \geq 0.01$ and $T_e/T_{sine1} \leq 2.5$ can be examined.

5.5.2 Influence of Q_1 and Q_2 on $1/\alpha'$, $1/\alpha''$, f_d', f_d'', $|r'|$, $|r''|$, θ' and θ''

1) Influence of Q_1

Method

Use the same parameters as in Eq. 5.5, except that, rather than a fixed value, Q_1 is assigned to 30, 50, and 100 respectively.

Next, sample k between $0.01 \leq k \leq 0.16$, replace the parameters in Eq. 5.3, by the corresponding parameters in Eq. 5.5, and calculate the poles and residues in Matlab for each k. Similar to the method in section 5.2.1, the relations of $1/\alpha'$ and $1/\alpha''$ versus k, f_d' and f_d'' versus k, $|r'|$ and $|r''|$ versus k, and θ' and θ'' versus k are plotted in Fig. 5.13 A, B, C and D.

Results

Fig. 5.13 demonstrates the following points:

Regardless of the changes to Q_1, $1/\alpha'$, $1/\alpha''$, f_d', f_d'', $|r'|$, $|r''|$, θ', θ'' show similar features as before along the k axis. Their characters are still distinguished by the three k regions described in section 5.2.1, but the positions of the three k regions are influenced by Q_1.

The most noticeable influence of Q_1 is on the damping constant $1/\alpha'$ when the coupling is weak ($k < 0.04$). If Q_1 is large, $1/\alpha'$ is large. Its effect on the modulation waveform is that the duration of the modulation lasts longer at weaker coupling.

2) Influence of Q_2

Method

Similarly, sample k between $0.01 \leq k \leq 0.16$; let Q_2 equal 10, 20 and 30 respectively in Eq. 5.5 and the other parameters unchanged; replace the parameters in Eq. 5.3 by the corresponding values; plot the relations of $1/\alpha'$ and $1/\alpha''$ versus k, f_d' and f_d'' versus k, $|r'|$ and $|r''|$ versus k, θ' and θ'' versus k in Fig. 5.14 A, B, C and D.

Results

Again, regardless of the different values of Q_2, the development of $1/\alpha'$, $1/\alpha''$, f_d', f_d'', $|r'|$, $|r''|$, θ', θ'' along the k axis follows the same patterns as that already described. However, Q_2 affects the positions of the three k regions.

Compared to Q_1, Q_2 has a stronger influence on these parameters, most obviously on $1/\alpha'$, $1/\alpha''$, $|r'|$ and $|r''|$. When Q_2 is greater, $1/\alpha''$, $|r'|$ and $|r''|$ increase, and $1/\alpha'$ is also greater after $1/\alpha'$ and $1/\alpha''$ cross each other in Fig. 5.14 A. Such changes are likely to affect all the aspects concerning a modulation waveform: duration, amplitude and shape (beating).

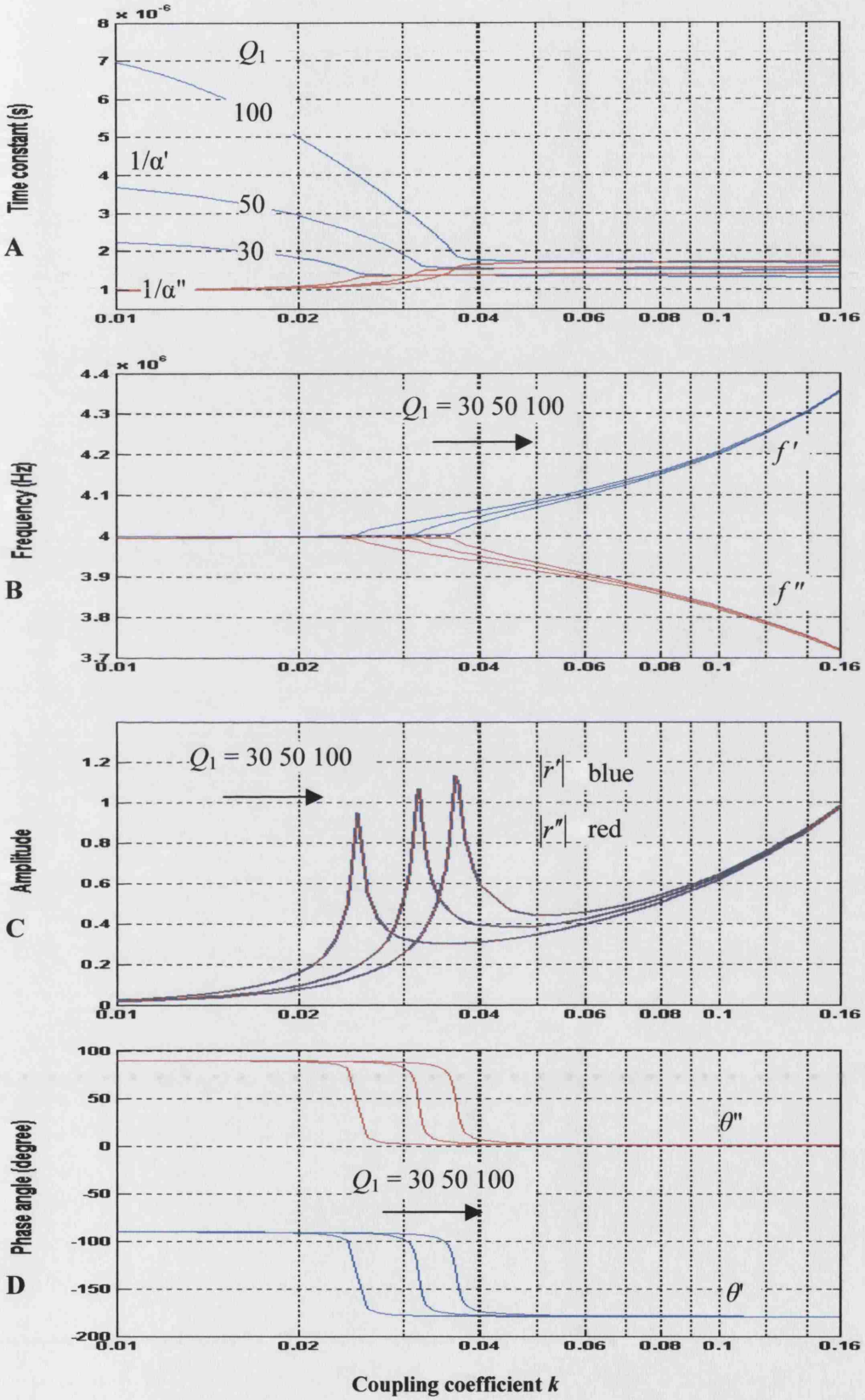


Fig. 5.13 Influence of Q_1 on the parameters of the modulation waveform.

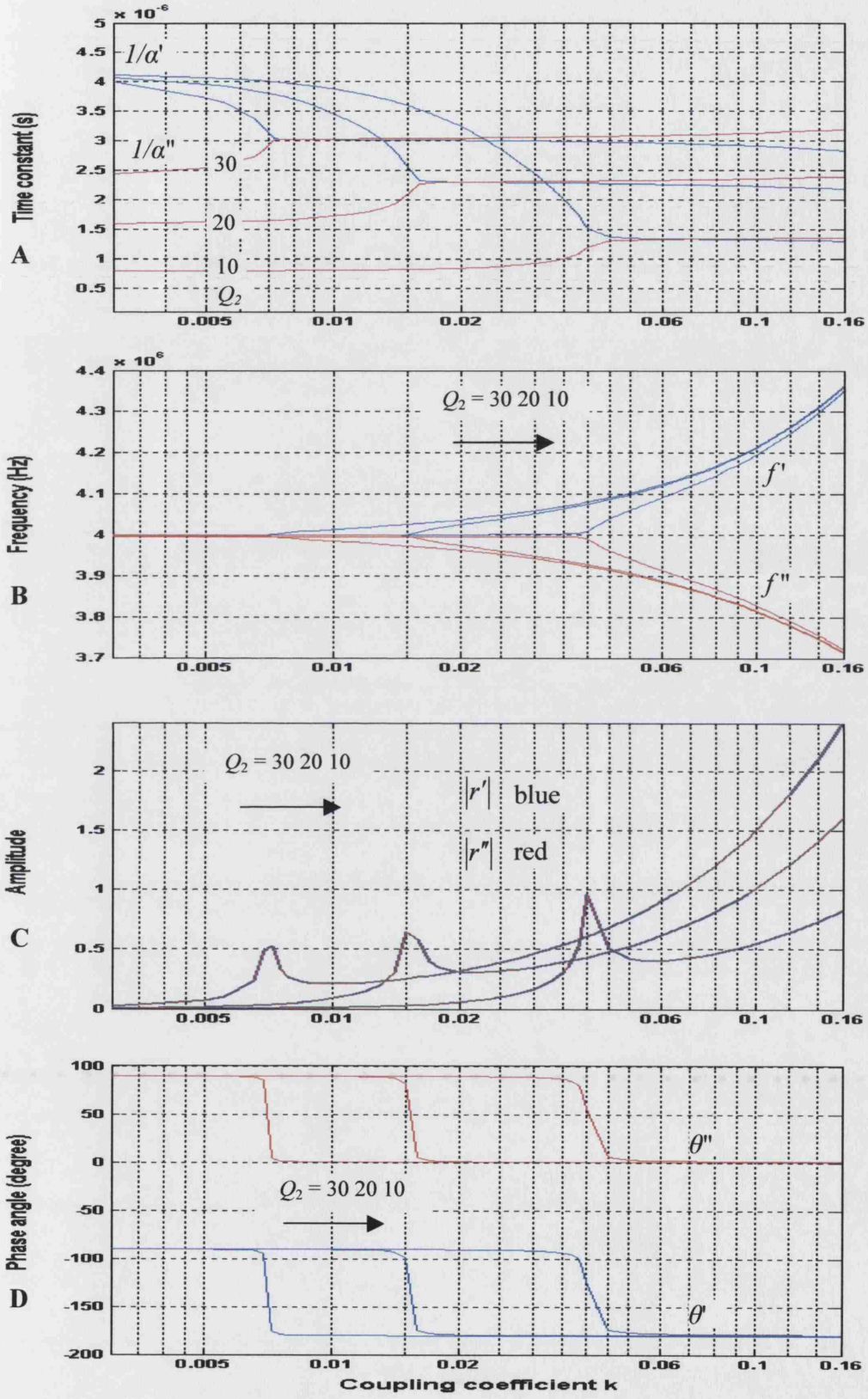


Fig. 5.14 Influence of Q_2 on the parameters of the modulation waveform.

3) Summary of the influence of Q_1 and Q_2 on $1/\alpha'$, $1/\alpha''$, f_d', f_d'', $|r'|$, $|r''|$, θ' and θ''

The development of $1/\alpha'$, $1/\alpha''$, f_d', f_d'', $|r'|$, $|r''|$, θ' and θ'' along the k axis is always characterised by the three distinct k regions, no matter what the values of Q_1 and Q_2. Hence, the modulation waveform will be expected to progress in a similar manner to that discussed in section 5.3: it is a small single ramp at the weaker coupling, and beats when the coupling reaches a greater value; in between, the waveform is large enough to be detectable, yet without obvious beating. This is the k working range which is suitable for PPSM.

Q_1 and Q_2 affect the position of the three k regions and the individual parameter, with the influence from Q_2 being stronger than that from Q_1. This will result in a move of the k working range. As discussed, the lower boundary of the k range is indicated by the modulation index, and the upper boundary by the Te/Tsine1 ratio. The k working range regarding the variation of Q_1 and Q_2 values will be examined next.

5.5.3 Influence of Q_1 and Q_2 on the k working range

1) On the lower k boundary

Firstly, calculate the modulation index m. The procedure is as follows: let Q_1 be one of {30, 50, 100}, and Q_2 be one of {10, 20, 30}; sample k between 0.005 to 0.16, and let f_0 = 4 MHz; replace the parameters in Eq. 5.3 by these corresponding values, and calculate the poles and residues in Matlab for each k; construct $i_{1natural}$ by Eq. 5.4, and find its maximal amplitude in Matlab; calculate the modulation index m by Eq. 5.25, and plot the results in Fig. 5.15.

Fig. 5.15 demonstrates that Q_2 has a greater impact on the m compared to Q_1. When the k is given, higher Q_1 and Q_2 both lead to higher m, but the influence of Q_2 is dominant. This means that when Q_2 is large, even at a very weak coupling, the modulation is still detectable; so the lower boundary of the working k is extended to a smaller value.

The shaded area in Fig. 5.15 marks the place where m ≤ 0.01. If a modulation index curve falls into the area, the corresponding modulation is undetectable. For example, for Q_2 = 10, the modulation becomes undetectable when the k is less than about 0.013; for Q_2 = 20, the k boundary is around 0.007; for Q_2 = 30, it is around 0.005.

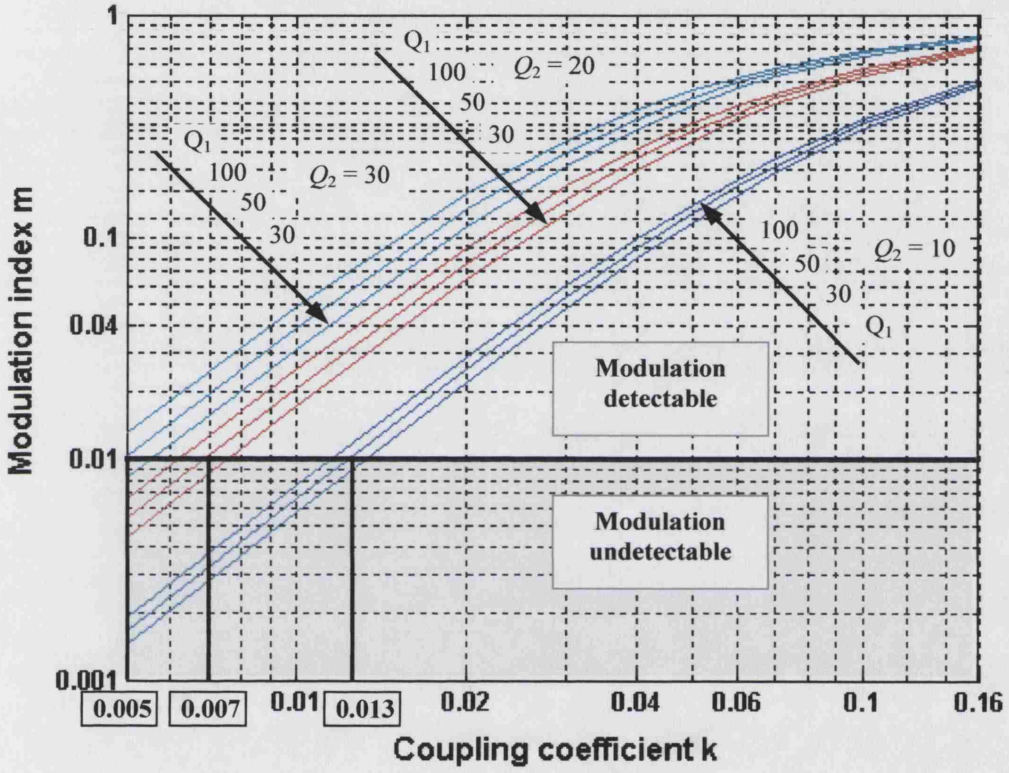


Fig. 5.15 Influence of Q_1 and Q_2 on the modulation index.

2) On the upper *k* boundary

Firstly, calculate the T_e/T_{sin1} ratio. As before, let Q_1 be one of {30, 50, 100}, and Q_2 one of {10, 20, 30}; sample k between $0.005 \le k \le 0.16$, and let f_0 = 4 MHz; substitute the parameters in Eq. 5.3 with these values, and calculate the poles in Matlab for each k. Hence, α' and α'' (the real part of the poles), and ω' and ω'' (the imaginary parts) are known. Next, calculate the T_e/T_{sin1} by Eq. 5.11 and Eq. 5.12, and plot the results in Fig. 5.16.

Fig. 5.16 shows that Q_2 again has a greater impact on the T_e/T_{sine1} ratio compared to Q_1. Higher Q_1 and Q_2 both lead to a high T_e/T_{sine1} ratio, but the influence of Q_2 is dominant. Because $T_e/T_{sine1} \geq 2.5$ indicates the appearance of beating, having a high Q_2 means the waveform tends to beat even when the coupling is not strong; the upper boundary of the working k, hence, moves to a smaller value.

The shaded area in Fig. 5.16 marks the place where $T_e/T_{sine1} \geq 2.5$. If a curve falls into the area, the corresponding waveform beats, suggesting it is unsuitable for PPSM. For example, for $Q_2 = 10$ this upper k boundary is around 0.18; for $Q_2 = 20$ it is around 0.115; for $Q_2 = 30$ is around 0.08.

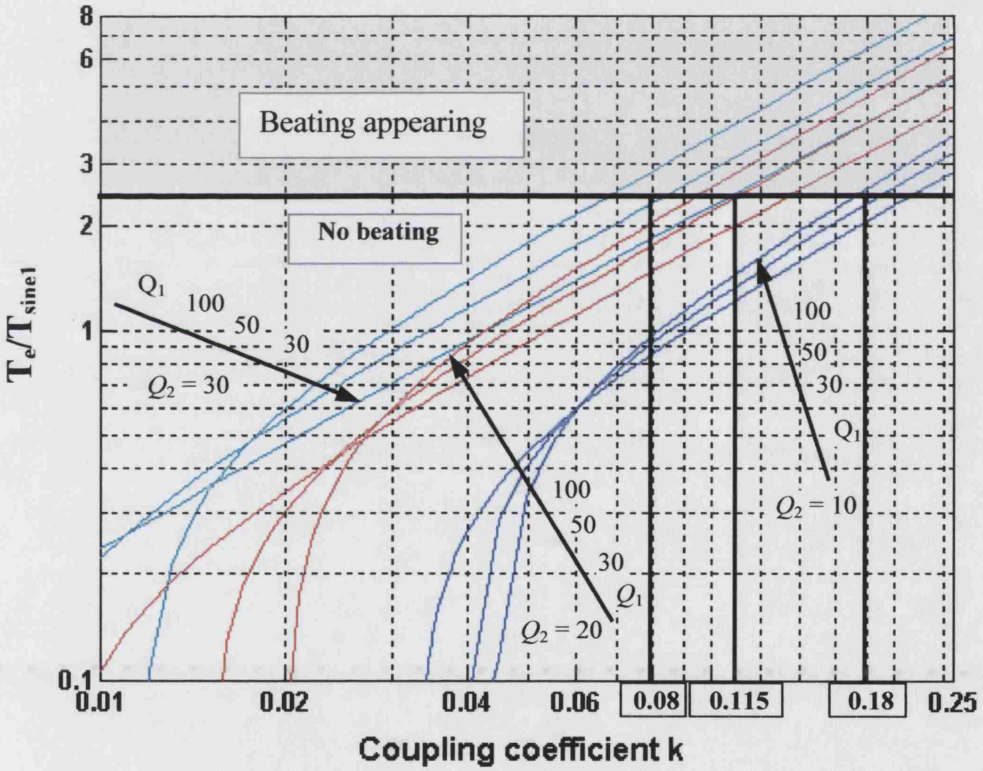


Fig. 5.16 The influence of Q_1 and Q_2 on the modulation waveform.

3) On the working *k* range

Fig. 5.17 summarizes the k working range under the different values of Q_1 and Q_2. The blue, red, and green bars mark the k working range when Q_2 equals 10, 20 and

30 respectively. The lighter shaded areas at both ends of the bars indicate the differences caused by Q_1, varying from 30 to 100.

The figure shows that Q_2 is the major factor affecting the k working range. When Q_2 is high, the working k range moves towards lower values; when it is low, the working k range moves to higher values. In other words, if the quality factor of the secondary circuit is given and the coupling range is known, the suitability of PPSM can be estimated from the figure.

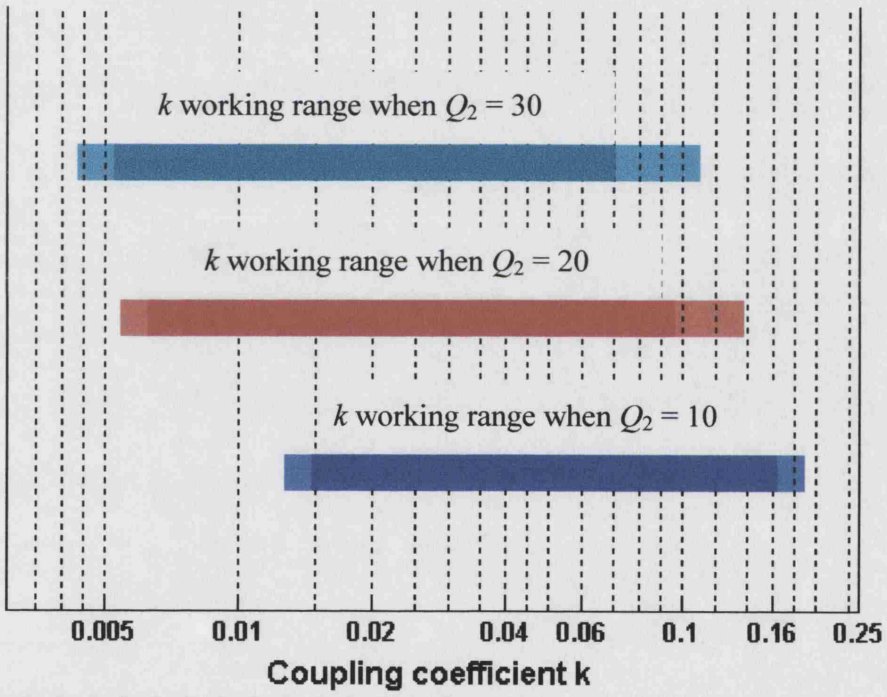


Fig. 5.17 The k working range at various values of Q_1 and Q_2. The lighter shaded areas at both ends of the bars indicate the differences caused by Q_1 varying from 30 to 100.

5.5.4 The influence of Q_1 and Q_2 on the modulation duration

Another concern is how Q_1 and Q_2 affect the modulation duration, and thus the achievable bit rate. It will be examined by finding the relation of Q_1 or Q_2 with $1/\alpha'$, as the modulation duration is approximately five times $1/\alpha'$.

Firstly, plot $\frac{1/\alpha'}{T_0}$ versus k curves under various values of Q_1 and Q_2. Let Q_1 be one of {30, 50, 100}, and Q_2 one of {10, 20, 30}; sample k between $0.005 \leq k \leq 0.16$, and let f_0 = 4 MHz, $T_0 = 1/f_0$; substitute the parameters in Eq. 5.3 by these values, and calculate the poles in Matlab for each k. Hence, α' (the real part of one of the poles) is obtained. Let $\frac{1/\alpha'}{T_0}$ be the normalised time constant, and plot $\frac{1/\alpha'}{T_0}$ versus k in Fig. 5.18. Repeat the above procedure for all nine Q_1 and Q_2 combinations.

It is easy to assume that the modulation would last longer for a high Q circuit because it is less damped. However, as there are two Qs in the coupled circuits, the duration problem is more complicated, as shown in Fig. 5.18.

At a smaller k, Q_1 is the major factor to affect the duration: a larger Q_1 gives a longer time constant or duration. At a greater k, Q_2 is the major factor: a larger Q_2 generally gives a longer duration. In between, it is more uncertain. For example, the circuit with $Q_1 = 50$ and $Q_2 = 10$ (the curve marked with "50, 10") has a longer duration at $k \leq 0.03$ than the circuit with $Q_1 = 50$ and $Q_2 = 20$ (the curve marked with "50, 20").

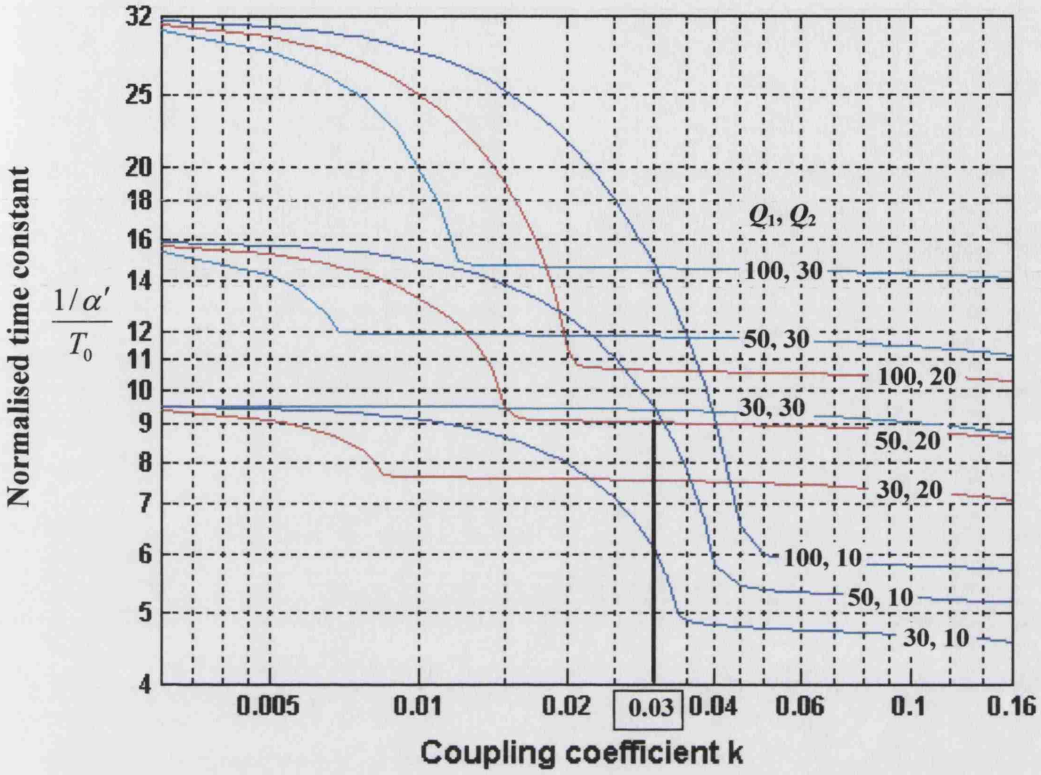


Fig. 5.18 The influence of Q_1 *and* Q_2 *on the normalised time constant* $\frac{1/\alpha'}{T_0}$

From Fig. 5.18, the modulation duration can be estimated. For example, given f_0 = 4 MHz, Q_1 = 53 and Q_2 = 12, from the curve marked with "50, 10", we know that the normalised decay time constant in $0.01 \leq k \leq 0.16$ is between $5.2 \leq \frac{1/\alpha'}{T_0} \leq 15$ so that the duration will be $5 \times 5.2 / f_0 \sim 5 \times 15 / f_0$, which is 6.5 μs ~ 18.75 μs. In our application, a new data bit can be applied after this duration finishes. But this will result in a slower bit rate. It is often feasible by applying the next bit in a shorter time interval in order to achieve a faster bit rate. In the above example, the interval between two adjacent bits is set at 4.5 μs, making the bit rate 222.2 kbit/s. The justification for this is as follows: Fig. 5.18 suggests that the duration becomes longer as k decreases. So the worst case in terms of estimating the bit rate happens when k is small (say k = 0.02). Given the same parameters as the above example, Fig. 5.2 demonstrates how the modulation waveform is composed by the two damped sine waves at k = 0.02. The peak

of the compound waveform occurs after the amplitude of the shorter damped sine wave is significantly reduced at about 2 μs, which is 2 × 1/α" (the shorter decay time constant, see Fig. 5.1 A). By 4.5 μs, the amplitude (green curve) decreases to 60% of the peak level. From simulation and experimental test, we know this amplitude difference is big enough to distinguish a modulation. Hence, the 4.5 μs bit interval is chosen.

5.6 Summary

This chapter has analysed the circuit response of i_1 in stage 3. The i_1 function is derived according to the properties of 1/α', 1/α", f_d', f_d", $|r'|$, $|r''|$, θ' and θ" along the k axis.

The transient response generated in this stage is the PPSM response. Its amplitude increases with the coupling. Its waveform has a single peak for most of the coupling range, but shows the beat phenomenon at the higher values of k. Its duration is determined by 1/α'.

A detectable, no beating or no obvious beating waveform is judged as suitable for representing a modulation. The detectability is indicated by the modulation index m; it defines the minimal k for PPSM to work. The beating phenomenon can be predicted from the T_e / T_{sine1} ratio. The coupling at which the beating starts defines the maximal k for PPSM to work. Between the minimal k and the maximal k is the PPSM working range.

Q_1 and Q_2 affect the working range but Q_2 has a more significant influence. Having greater values of Q_1 and Q_2, the modulation tends to work at higher k values and vice versa. If Q_1 and Q_2 are known, a suitable working range for PPSM can be estimated from Fig. 5.17.

Q_1 and Q_2 affect the modulation duration in a complicated manner. Given Q_1 and Q_2, the duration can be evaluated from Fig. 5.18.

In Chapter 2, we have the typical circuit parameters for the RF link of our concern, which are as follows: Q_1: 30 ~ 100, Q_2: 10 ~ 30, k: 0.01 ~ 0.16. From Fig. 5.17, we can conclude that the hypothesis, which states that the transient waveform

generated by PPSM is in good shape for demodulation within the required working ranges, is generally true, except that the working range moves a little along the k axis.

In particular, the circuit parameters optimised for efficient power transmission for the k range 0.01 ~ 0.16 also allow PPSM to work optimally. Therefore, the hypothesis 5 suggested in Chapter 1, that the circuit parameters optimised for power transfer efficiency are also good for signalling, is also true.

A method for analysing the transient response of forth order magnetically coupled circuits is developed in the latest two chapters. The procedure includes identifying the modulation stages, establishing the initial conditions, simplifying the multi-inputs problem to the single input problem, deriving $i_1(t)$ function, and analysing the circuit behaviour. Although the last two steps in the procedure are partly achieved numerically, they enable us to understand the cause of the modulation, the components of the modulation waveform, the development of the waveform regarding to variables k, Q_1, and Q_2. And we are able to predict the working range. From this point of view, the method serves the same purpose as a pure analytical solution does. Therefore, it is a generic method and adaptable for solving similar problems.

The next part of the thesis will discuss the electronic design for implementing PPSM, in order to demonstrate the validity of the PPSM theory.

Part 3

System Design

Chapter 6 PPSM system design – Overview and The transmitter

6.1 Introduction

The next three chapters will present the design of an electronic system for implementing *Passive Phase Shift Modulation*. There are two aims: to demonstrate that PPSM works in a real system, and to construct a PPSM prototype which could be adopted by the implantable neuroprosthesis discussed in Chapter 1.

The specific task is to convey two channels of analogue signal, each having a 5 kHz bandwidth, from a circuit representing an implant to a circuit representing an external side via a pair of coupled coils by PPSM. The carrier is 4 MHz, the data rate is 222.2 kbit/s. For both power and data transmission, the working coil-coil spacing should be up to 70mm.

6.2 System overview

The principle of PPSM is illustrated in Fig 4.1, Chapter 4. The components for the power transmission are included in the figure, and their optimal values are given in Chapter 2. However, in order to permit data transmission, several expansions in Fig 4.1 are necessary, and they are illustrated in Fig. 6.1.

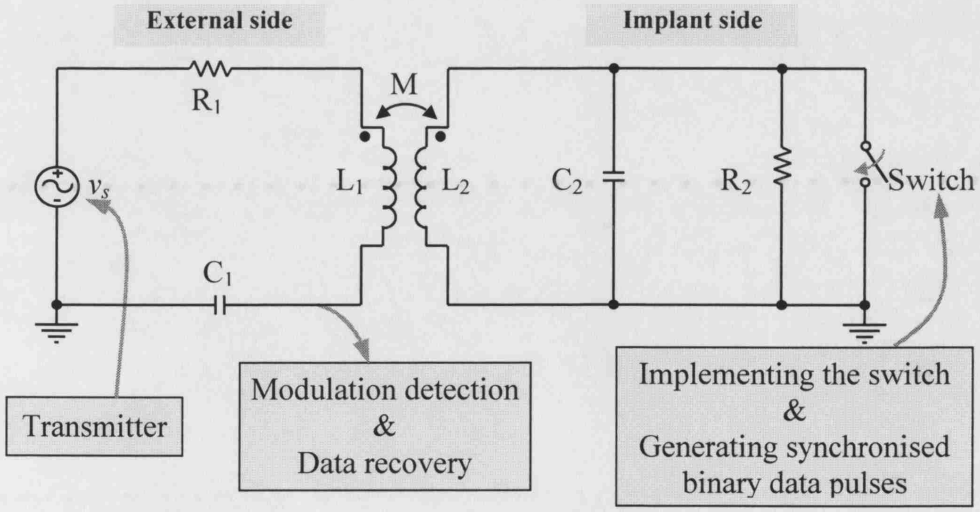


Fig. 6.1 Additional designs needed to realise PPSM.

First of all, a power transmitter is needed to act as the external source v_s. At the implant side, it needs a means to implement the switch, and to generate synchronised binary data pulses to control it. At the external side, the modulation has to be detected and recovered back to the usual data format. Furthermore, a strategy for word reconstruction has to be designed; in other words, it needs an encoding and decoding method.

Fig. 6.2 is an overview of the system. It comprises an implant board, an external board, a transmitter board, a pair of coils and a battery.

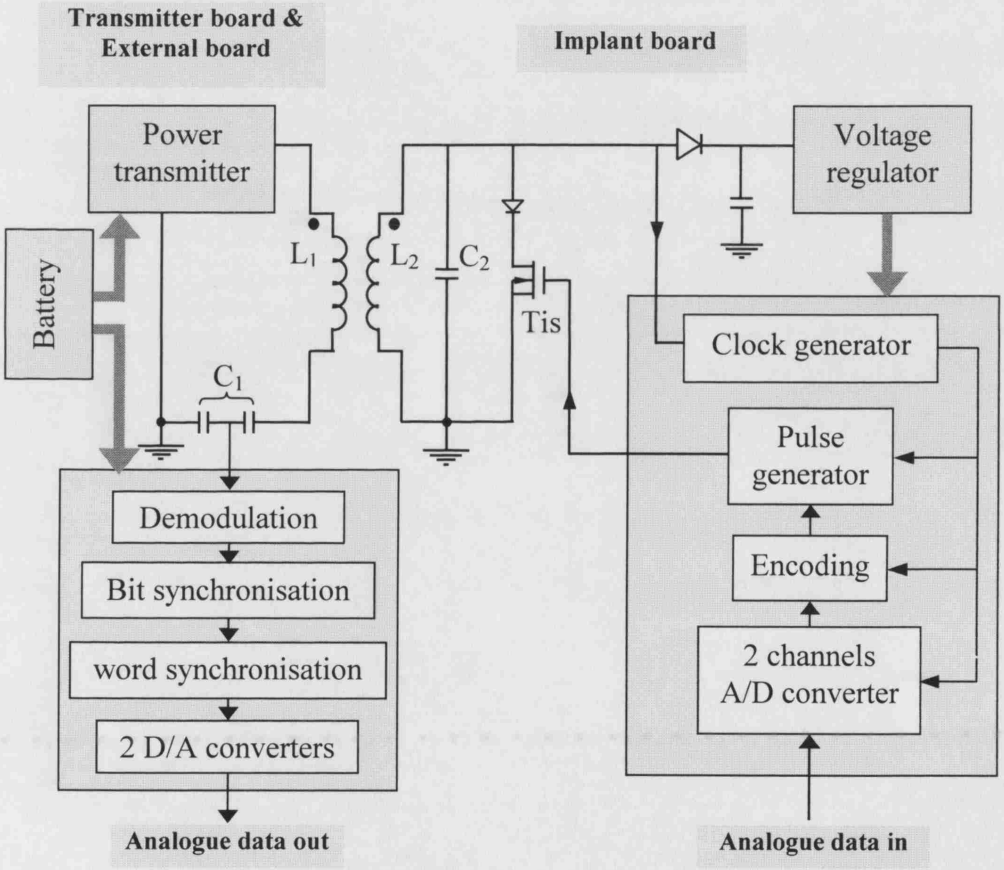


Fig. 6.2 The PPSM system overview

The power transmitter will drive the L_1C_1 circuit, sending the 4 MHz RF to the implant. On the implant board, the RF is received, rectified, smoothed and regulated to a DC voltage. There are two analogue signals to the A/D converter input, each of which is sampled at 10 kHz with 10 bits resolution. The digital bits are then encoded and

converted to a synchronised pulse train to control the switch. The switch is implemented by an FET in series with a diode. On the external board, the modulation is extracted from a capacitor voltage divider. After demodulation, bit synchronisation and word synchronisation, the digital format of the data is recovered. The digital data are then converted back to analog signals by two D/A converters.

6.3 Design consideration and technology

The system will be constructed at board level. Digital logic circuits on both the implant and external sides will be implemented into CPLDs[1] by VHDL[2] in order to reduce the size of the circuit board, and to make it easier to convert the design to custom produced ICs if necessary. Off-the-shelf ICs and discreet components will be used in the rest of the system. The design will emphasise simplicity and low power to suit the requirements of the implant and portable device.

6.4 The author's contributions

The implant and external circuits were designed by the author. The transmitter is a modified version of Tim Perkins' design for the LARSI[3] system [77]. The transmitter will be described next in this chapter. The implant and external circuits will be discussed in Chapter 7 and 8 respectively.

6.5 Transmitter

Fig. 6.3 is the schematic diagram of the transmitter. Fig. 6.4 is the transmitter circuit board. The circuit consists of two major parts: to the left of the transformer are a master oscillator and the buffers; to the right is a class-D type power amplifier.

The master oscillator is constructed by a quartz crystal CTt, resistors R_{t1} and R_{t2}, and a CMOS inverter U_t/A. The oscillation frequency is set at 4 MHz by the crystal CTt. After being buffered by U_t/B U_t/C, U_t/D, U_t/E and U_t/F, the output of the oscillator

[1] Complex Programmable Logic Device.
[2] VHSIC Hardware Description Language, VHSIC is an abbreviation for Very High Speed Integrated Circuit.
[3] Lumbar Anterior Root Stimular Implant

drives the transformer's primary winding. The oscillator and buffers operate on a 5V supply, Vtcc1.

The step-up transformer converts the voltage level from ±2.5V to ±5V. The two secondary windings of the transformer have equal turns but in opposite directions. Thus, the voltages driving the gates of T_{t1} and T_{t2}, and the gates of T_{t3} and T_{t4} have 180° phase difference, making T_{t1}, T_{t2} and T_{t3}, T_{t4} conduct alternatively, and forming a push-pull output. T_{t1} and T_{t2} are used in parallel in order to increase the FET's capability of handling larger current; such arrangement also reduces the output impedance (the "ON" resistance). For the same reasons, T_{t3} is in parallel with T_{t4}.

L_1 is the primary coil discussed in the preceding chapters. Its value is given in Chapter 2, 19.9μH. The required tuning capacitance is 79.6pF for 4 MHz. It is formed by C_{t2} ~ C_{t6}, a capacitor network which makes the total capacitance vary between 69pF ~ 87pF. C_{t2} ~ C_{t5} and C_{t6} also form a voltage divider. The modulation will be extracted from the voltage on C_{t6}.

The class D power amplifier is supplied by Vtcc2. Vtcc2 determines the amplitude of the external source, v_s, discussed in the previous chapters. It is preferable that Vtcc2 is variable in relation to the coupling. The reason is as follows: at the implant side, the minimal peak-peak voltage across the receiver coil is required to be greater than 7.72V (see Section 7.2); and in order to limit the energy loss, it is better to maintain this voltage at this level regardless of the variation of the coupling so that the voltage drop across the implant regulator is kept small all the time. Although an effort has been made to stabilise the receiver voltage by optimising the circuit parameters (for example, using an external coil larger than the implant coil, and making the link to work around the critical coupling, see Chapter 2), letting Vtcc2 compensate the coupling variations will achieve a further stabilisation, see below:

From Eq2.17, Eq. 2.8 and Eq. 2.9 in Chapter 2, we have

$$E = \frac{\sqrt{(1+k^2Q_1Q_2)^2 + k^4Q_1^2}}{\sqrt{\frac{L_2}{L_1}}\, kQ_1Q_2} V_{C2\max} \qquad \text{------ Eq. 6.1}$$

in which E is the amplitude of the external source v_s discussed in the previous chapters. V_{C2max} is the amplitude of the receiver voltage, and here, it is 7.72V; Q_1, Q_2, L_1 and L_2 are known parameters. Therefore, each k corresponds to an E.

In Fig. 6.3, the output of the FETs is a square waveform, switching between the ground and Vtcc2. Represented by the Fourier series, this square waveform is $f(t) = \sum_{n=1}^{\infty} \frac{2\,Vtcc2}{\pi n} \cos(n\omega t)$. Because the $L_1C_{t2\sim6}$ circuit in the figure is series-tuned at 4MHz and has high Q, the odd harmonics (even for the 3rd one) are attenuated significantly. Therefore, the square wave source can be approximated by the sinusoidal wave of the fundamental frequency: $f(t) \approx \frac{2\,Vtcc2}{\pi} \cos(\omega t)$. The amplitude $\frac{2\,Vtcc2}{\pi}$ then corresponds to E in Eq. 6.1. So, in order to keep V_{C2max} at 7.72V in the receiver side, the relation between k and Vtcc2 is:

$$Vtcc2 = \frac{\pi}{2} \frac{\sqrt{(1+k^2 Q_1 Q_2)^2 + k^4 Q_1^2}}{\sqrt{\frac{L_2}{L_1}}\, k Q_1 Q_2} V_{C2\max} \qquad \text{------ Eq. 6.2}$$

Letting Eq.2.11 be divided by Eq.2.17 gives

$$k = \sqrt{\frac{L_2}{L_1}} \frac{V_{C2\max}}{R_2} I_{1\max} \qquad \text{------ Eq. 6.3}$$

where I_{1max} is the amplitude of the primary current. By measuring the primary current, we shall know the degree of the coupling, and thus the required Vtcc2.

This idea is used in the LARSI system. Perkins [77] describes its electronic design. In the author's bench system here, however, it is not implemented. Instead, varying Vtcc2 is achieved by manually adjusting the power supply voltage because the main aim here is to validate PPSM.

The chosen FETs in Fig. 6.3 are BS170 [13] (Philips Semiconductors). This transistor has a switching on time t_{on} = 10 ns, and off time t_{off} = 10 ns, which is capable of handling 4 MHz; and its voltage and power ratings are suitable for this application.

High voltage capacitors with low ESR are required for $C_{t2} \sim C_{t6}$. The maximum voltage on the capacitors is expected to be around 300V.

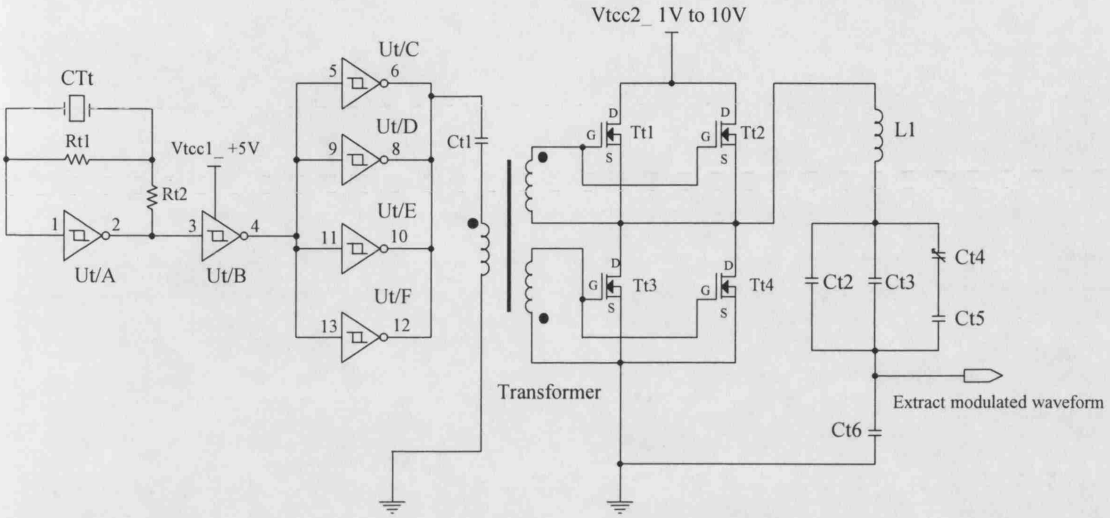


Fig. 6.3 Schematic diagram of the transmitter circuit

Notes on Fig. 6.3:

1. Two voltage supplies: Vtcc1: 5V; Vtcc2: variable, 1V~10V.
2. CTt: crystal resonant at 4 MHz.
3. IC: U_t is HEF74HC14 from Philips Semiconductors.
4. FETs: T_{T1}, T_{T2}, T_{T3} and T_{T4}: BS170 from Philips Semiconductors.
5. Transformer: ferrite pot core B65511 from Siemens.

   Primary: 10 turns

   Secondary: 20 turns

   Third: 20 turns

6. Other component values

Component	Value
C_{t1}	100 nF
C_{t2}	22 pF
C_{t3}	22 pF
C_{t4}	60-500 pF
C_{t5}	47 pF
C_{t6}	820 pF
R_{t1}	1 MΩ
R_{t2}	220 Ω
L_1	19.9 μH

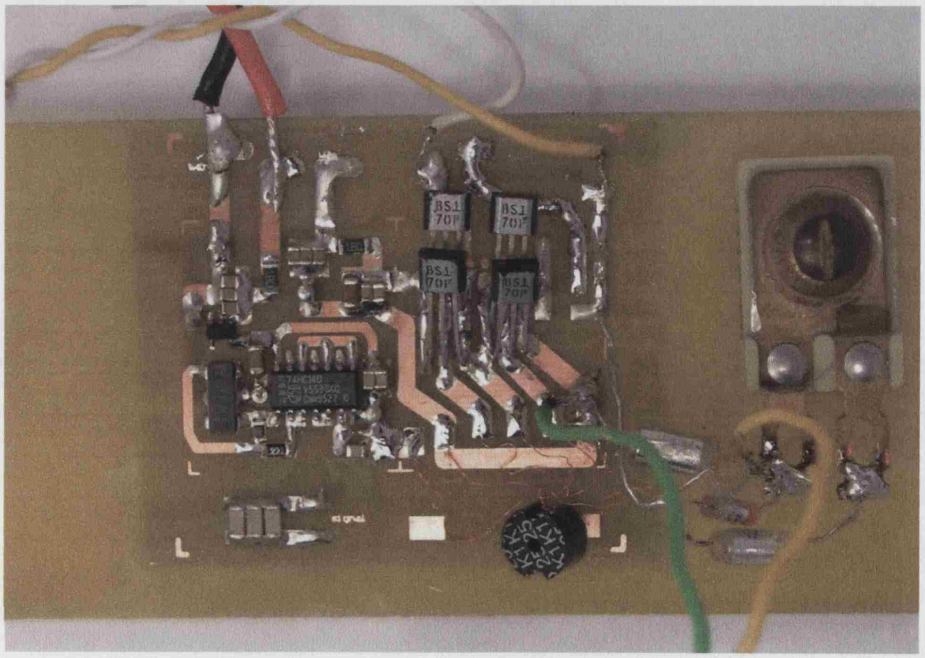


Fig. 6.4 Transmitter circuit board

Chapter 7 PPSM system design – The implant circuit design

7.1 The implant circuit overview

The tasks of the implant circuit are: to receive and convert the 4 MHz RF to DC voltages to supply the implant electronics; to sample and digitise the analogue signals, encode the sampled data, and output them as synchronised pulses to control the modulation switch. A clock generated from the RF paces the logic process.

Fig. 7.1 is an overview of the implant circuit.

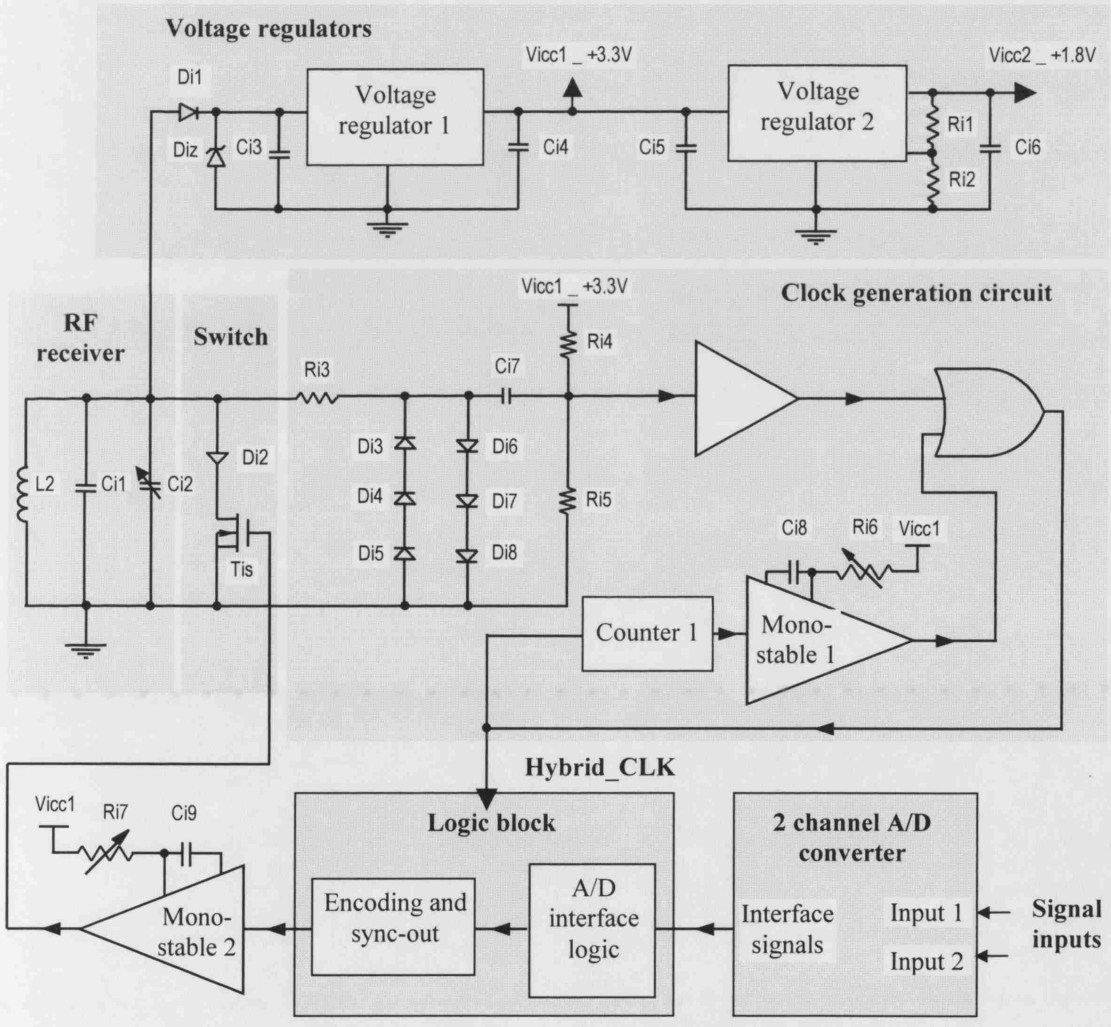


Fig. 7.1 An overview of the implant circuit.

It consists of an RF receiving circuit, two DC voltage regulators, a clock generation circuit, a logic block for A/D interfacing, encoding and synchronisation, a two channel A/D converter and a switch. They will be described next.

7.2 The RF receiving circuit and DC supplies

L_2, C_{i1} and C_{i2} are tuned to resonate at 4 MHz, picking up the RF[1]. After being rectified and smoothed by D_{i1} and C_{i3}, the RF is converted to +3.3V and +1.8V by two voltage regulators. Vicc1 is +3.3V, and supplies part of the logic chip (the output drivers of the chip) and all the other components on the implant board; Vicc2 is +1.8V, and supplies the internal logic of the logic chip. The zener diode D_{iz} before the regulator is for protection.

Schottky diode BAT 85 [17] (Philips Semiconductors) is used as D_{i1}. It has low forward voltage (V_F = 0.32V at I_F = 1mA). The regulators are MAX604 [12] (Maxim Integrated Products). This IC features a low dropout (0.24V at 3.3V), large input ranges (2.7V to 11.5V), and an adjustable output; D_{iz}'s zener voltage is 11V.

The DC load of the implant circuit is estimated from the output current of regulator 1. When the circuit is working, its output current is measured as 3mA, resulting in R_{DC} = 3.3V/3mA = 1.1 kΩ. The equivalent AC load, which is the load looking into D_{i1} to the right, is 550Ω (see Chapter 2).

7.3 Clock generation

The clock generation (Fig. 7.2) follows three steps: generating a RawCLK, a blanking pulse and finally a Hybrid_CLK. The CLK stands for clock.

[1] The peak to peak voltage of the received RF should be greater than 7.72V (2 × (Diode forward voltage (0.32V) + Regulator dropout (0.24V) + Vicc1 (3.3V)), see later sections).

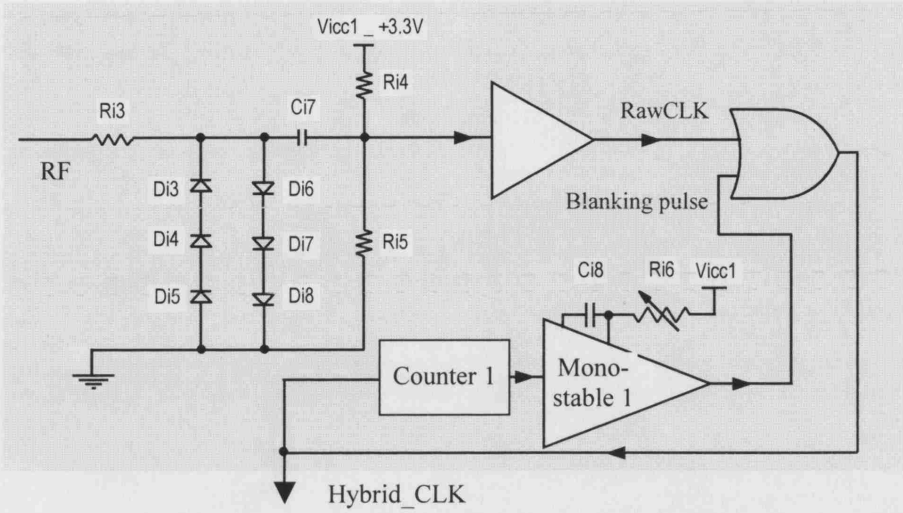


Fig. 7.2 Circuit diagram of the clock generation.

7.3.1 RawCLK

In order to synchronise the modulation pulses with the RF, a clock must be derived from the RF itself. The normal procedure is to reduce the RF amplitude to a logic level, and then feed it through a buffer, generating a square wave clock. This method is used here for generating RawCLK.

The circuit between the input RF and the output RawCLK in Fig. 7.2 is for this purpose. Diodes D_{i3}, D_{i4}, D_{i5}, D_{i6}, D_{i7} and D_{i8} limit the amplitude of the AC voltage to $3.75V_{peak\text{-}peak}$[2]. R_{i3} restricts the current flowing to the diodes and reduces the load for the coil. C_{i7}, R_{i4} and R_{i5} center the AC voltage at 1.65V DC ($V_{icc1}/2$). The signal at the buffer output is named RawCLK.

This part of the design focuses on choosing the proper components. They are selected according to two criteria: firstly, looking into R_{i3} to the right, the input impedance should be high compared to the input impedance to regulator 1, so that no significant amount of power is consumed by the clock generating circuit. Secondly, because the diodes have capacitance C_d in a practical situation, they form a low-pass

[2] 3× 0.625V = 1.875V at each direction, 0.625V is the diode forward voltage.

filter together with R_{i3} (see Fig. 7.3). In order not to attenuate the 4 MHz RF, R_{i3} and $D_{i3} \sim D_{i8}$ should be chosen so that the filter has a higher cut-off frequency.

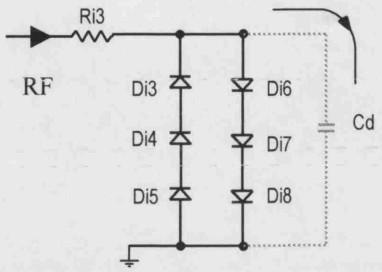


Fig. 7.3 R_{i3} and Cd making a low pass filter.

From the first criterion, a large value of R_{i3} is preferred. However, choosing a greater R_{i3} will result in a lower cut-off frequency for the filter ($f_{cut\text{-}off} = 1/(2\pi \times R_{i3} \times C_d)$). This problem can be partly compensated for by using diodes with a low C_d. Compared to zener diode and BAT85, IN4148 [21] (Fairchild semiconductor Corporation) has the lowest capacitance at 4 pF. It also has a large forward voltage drop 0.625V. Connecting six IN4148s as shown in Fig. 7.3 gives Cd = 2.67 pF, $V_{peak\text{-}peak}$ = 3.75V. If R_{i3} = 8 kΩ, then $f_{cut\text{-}off}$ = 11.9 MHz, which is beyond the RF frequency 4 MHz. 8 kΩ is also much larger than the input impedance of the DC supply (550Ω). The buffer will be implemented in the logic chip, and $V_{peak\text{-}peak}$ 3.75V is within the tolerance of its input.

7.3.2 Hybrid_CLK

Since the modulation interrupts the RF, some cycles may have smaller amplitudes or abnormal phases. The recovered RawCLK, therefore, has irregular intervals as shown by the third trace in Fig. 7.4. Such a signal is unsuitable as a clock. To overcome this problem, a long pulse (the fourth trace in Fig. 7.4) is used to blank the abnormal cycles. The relation is (RawCLK) OR (Blanking pulse) = Hybrid_CLK. The Hybrid_CLK (the fifth trace in Fig. 7.4) has a uniform pattern. It is used as the implant clock.

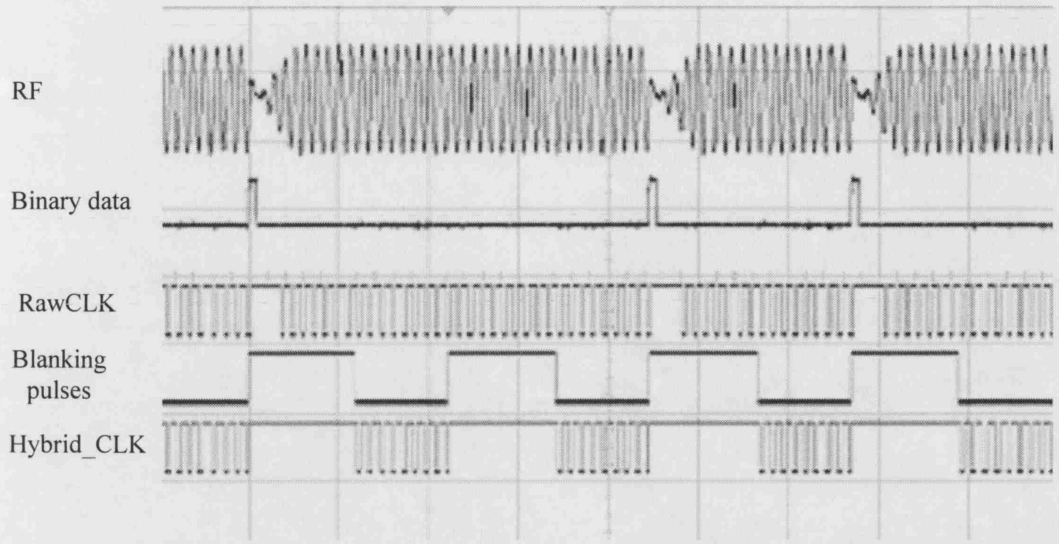


Fig. 7.4 Waveforms in the clock generation circuit

Fig. 7.5 shows the timing diagram for Hybrid_CLK generation. The timing and the pulse width of the Blanking pulses are set by counter 1 and the mono-stable in Fig. 7.2. Counter 1 counts on the rising edge of Hybrid_CLK, and recycles to 0 on reaching 8. In the first half cycle of clock No. 7, the counter outputs a Blanking_start pulse. The falling edge of the Blanking_start triggers the mono-stable to output a Blanking pulse. The Blanking pulse width is set by R_{i6} and C_{i8}, between 2500 ns to 2625 ns, which covers a period of 10 normal RF cycles. The Hybrid_CLK has a pattern of 8 normal clocks followed by a long pulse clock. The pattern repeats every 18 RF periods, that is 18×250 ns = 4.5 μs.

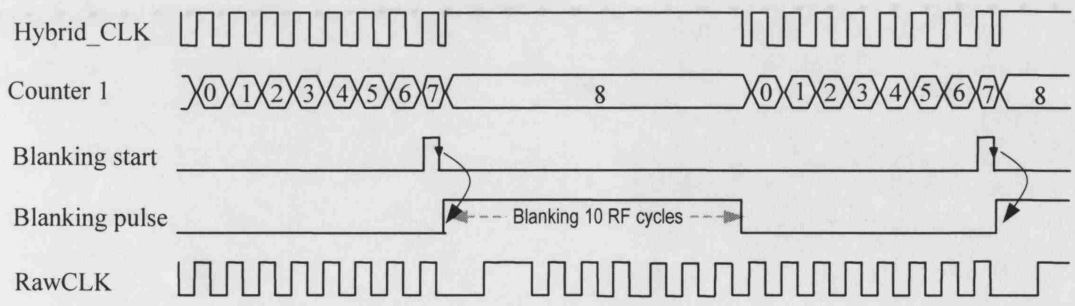


Fig. 7.5 Timing diagram for generating the Blanking pulse.

7.4 Logic block

7.4.1 Overview

The logic block generates the control signals for data acquisition, encoding and synchronised output. These operations are coordinated by the timing sequences derived from the Hybrid_CLK in order to achieve the required sample rate and transmission speed. The logic is written in VHDL and programmed into Coolrunner II XC2C64 [23], a CPLD from XILINX. Fig. 7.6 shows the diagram of the Logic block. It has several basic elements: 2 counters, a 20-bit register, two 1-bit registers P1 and P2, and an output buffer. Observing the Hybrid_CLK, it repeats a pattern of 8 short pulses followed by a long pulse. Counter 1 here is the same as the one in the clock generation circuit, and counts the individual Hybrid_CLK pulses within the pattern. It recycles to 0 when reaching 8. Counter 2 counts the number of patterns, and recycles 0 ~ 21. The timing of the command signals are derived from these two counters. These commands are for A/D interfacing and synchronised output, which will be discussed next.

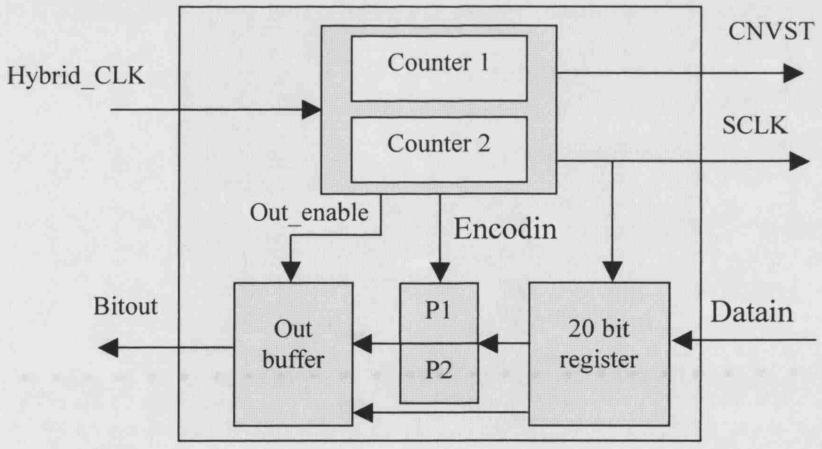


Fig. 7.6 Diagram of the logic block.

7.4.2 A/D converter interface

MAX1087 [19] (Maxim Integrated Products) is selected for sampling and digitising the analogue signals. It is a micropower, 10 bit, and 2 channel A/D converter having a serial output. The pinout and its interface with the logic circuit are shown in

Fig. 7.7. The A/D IC has two analog signal inputs, AIN1 and AIN2. It requires a conversion start signal CNVST and a serial clock SCLK from the logic circuit and sends the digital data to the DataIn port.

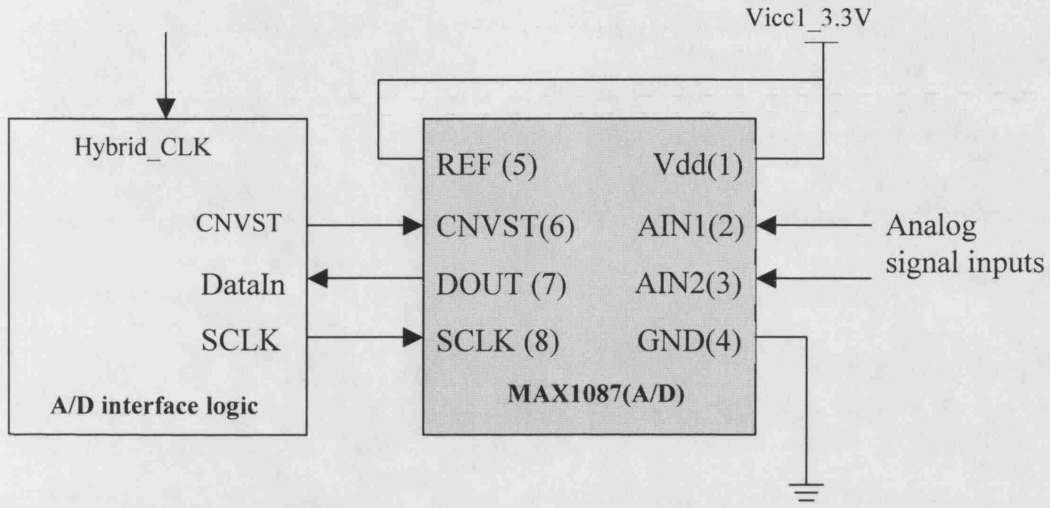


Fig. 7.7 A/D converter and its interface.

The CNVST and SCLK are formed according to the requirement of MAX1087. The timing diagram is illustrated in Fig. 7.8. When Counter 2 counts 0, a single pulse appears on the CNVST line. When it counts 11, twin pulses appear on the CNVST line. The different waveforms are for the selection of the input channel AIN1 or AIN2. Holding CNVST high for 2.5μs, the signal from channel 1 (AIN1) is acquired. Driving it low and waiting for 3.7μs, the conversion is completed, and the bit D9 is available at DOUT. At the rising edge of each SCLK, DOUT is read and stored in a 20-bit register in the logic block. At the falling edge of the SCLK, the next bit appears on DOUT. After 12 rising clock edges, 12 bits are read. Among them, the first 10 bits (D9 ~D0) are the data and the last two bits (S1, S0) are sub-bits which can be discarded in our application; hence, only D9 ~ D0 are stored in the register. Driving CNVST high for 250ns then low and high again, holding it for 2.5μs, the signal from channel 2 (AIN2) is sampled. The data are read as before.

The SCLK is kept low when the CNVST is active or when the conversion is in process. The low period is then followed by 8 clocks with wider pulse width and 4

clocks with narrower pulse width. Such an arrangement guarantees the 12 required SCLKs between the two CNVST signals so that all the data appearing on the DOUT are read once (although s0 and s1 are no use in this application, they must be read out. See the datasheet [19]).

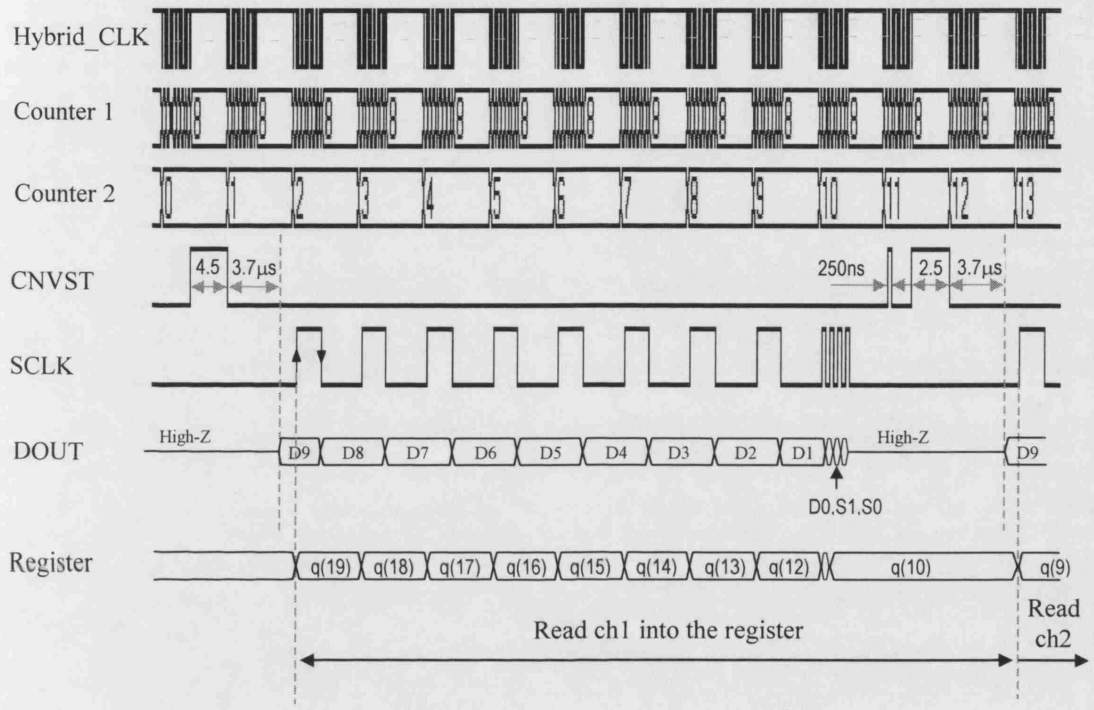


Fig. 7.8 Timing of the A/D interface logic

From Fig. 7.8, we see that in every 22-counts by Counter 2, each analog channel is sampled once. Because every count period contains one Hybrid_CLK pattern, each pattern is 18 RF periods long, so the sampling time is 22×18×250ns = 99000ns. This means each channel is sampled once every 0.099ms, resulting in a sample rate of 1/0.099ms = 10.1 kHz.

7.4.3 Encoding

Before they are sent out, the sampled data need to be encoded in order for the receiver to recognize them as a word frame in the bits stream.

A simple coding method is used: the 10 data bits from each channel are even parity checked, resulting in a parity bit. If P1 represents the parity bit for channel 1 and P2 for channel 2, the data and the coding bits are output in a sequence shown in Fig. 7.9. The most significant bit of channel 1 will first be output. Extracting the word frame at the receiver side will be discussed in the next chapter.

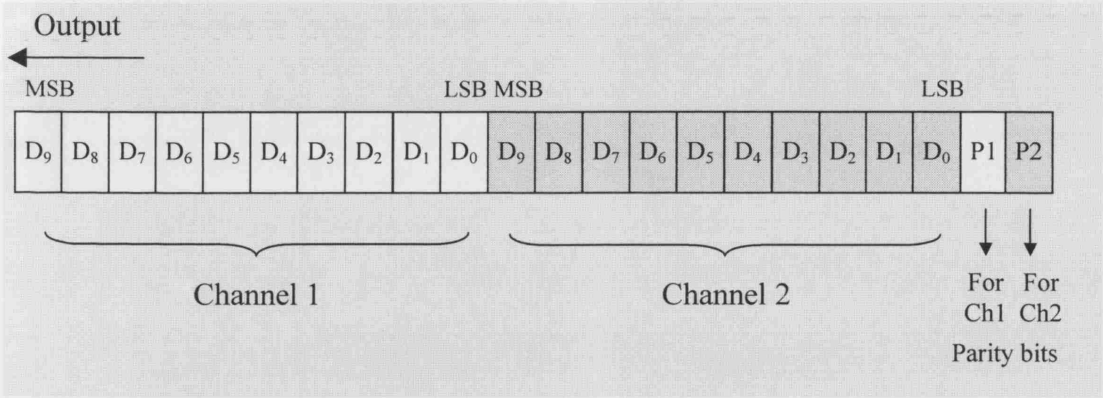


Fig. 7.9 Output sequence.

The reason to use even parity rather than odd parity is to improve the reliability of bit synchronization at the external side. Basically, the more transitions on the signal line, the less likely it will be out-of-sync (to be discussed further in Chapter 8). If all the 10 bits happen to be '0', the even parity check will output a '1' (Table 7.1), so that a very long sequence of '0's is avoided.

The reason to arrange P1 and P2 to append behind the data bits of the two channels is to identify the channels. Once the word frame is recognized, the first 10 bits will always be the data for channel 1, and the next 10 bits must be for channel 2.

Table 7.1 Definition of even and odd parity checking

Number of inputs of true 1	Parity check output	
	Even	Odd
0, 2, 4, 6, 8, 10	1	0
1, 3, 5, 7, 9	0	1

The encoding or the parity check is conducted immediately after the reading of the data is finished. The parity bits are saved in two one-bit registers, P1 and P2 (See Fig. 7.10, trace P1 and P2).

7.4.4 Bits output

Fig. 7.10 shows the output timing sequence. When Counter 2 counts 2, D9 from channel 1 is read into the register on the rising edge of SCLK. Two counts later, at the count No.4, D9 is loaded into Outbuffer by the 'load' command. When the 'Out_enable' signal goes high, it appears at 'Bitout' port. Similarly, when Counter 2 counts 5, D8 is outputted, and so on. By the time Counter 2 counts to 4 again, all 22 data and parity bits have been sent out. The logic block then starts to send the data from the next conversion.

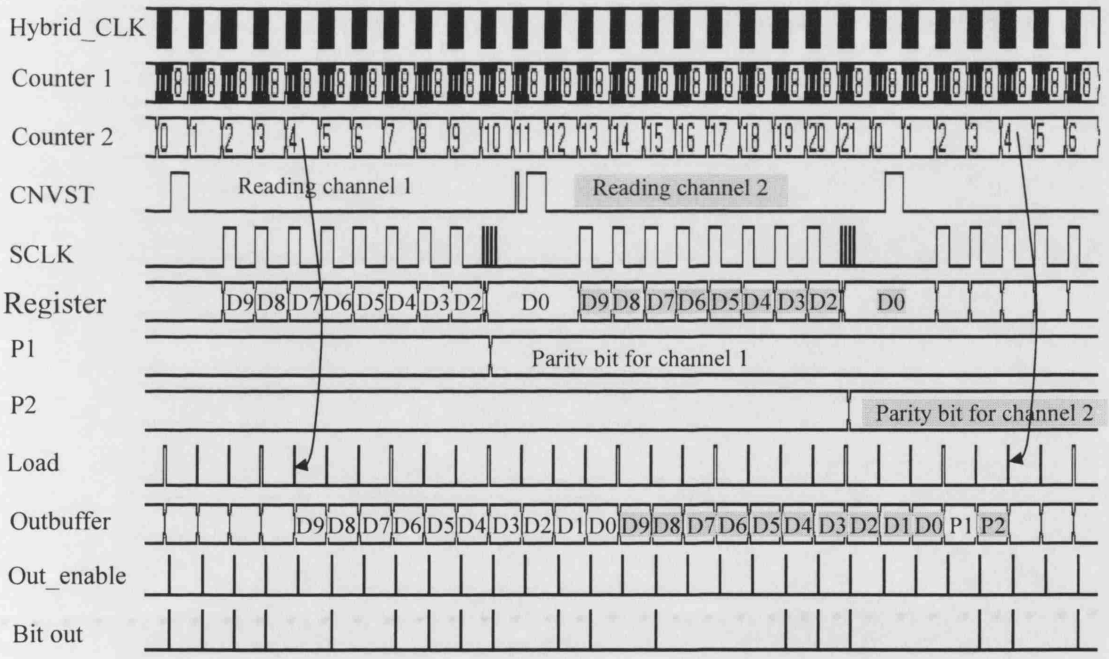


Fig. 7.10 Timing diagram of the bit output

An enlarged view of 'Load' and 'Out_enable' is shown in Fig. 7.11. The figure illustrates how the two signals have been derived from Counter 1 and Counter 2. The 'Load' becomes high on the count No.4 of Counter 1; the 'Out_enable' is high on count No.7, but only on the first half cycle. The Bitout is the same as

'Out_enable' if it is a '1'. Within each Hybrid_CLK pattern period, there is one 'Load' followed by one 'Out_enable'. This indicates only one bit is outputted.

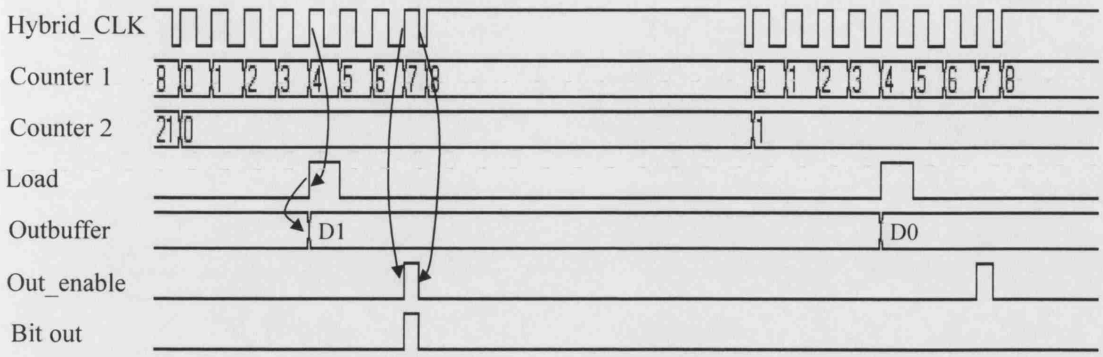


Fig. 7.11 Enlarged view of 'Load' and 'Out_enable' generation

7.5 Implementing the switch

Before discussing how to synchronously modulate the RF by the 'Bitout' signal, we shall look at how the switch is realised. The switch is implemented by an FET and a diode (Fig. 7.12). The bit pulses drive the FET's gate, and connect or disconnect the drain and source. The diode prevents reverse current flow if the FET is switched on at a negative half RF cycle. This allows greater tolerance of the switch timing.

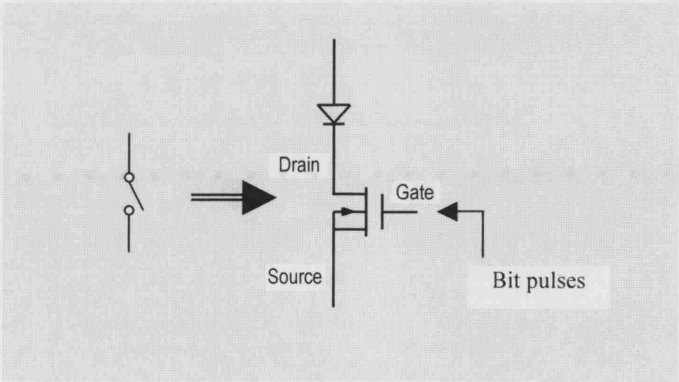


Fig. 7.12 Implementation of the switch

Selection of the components is based on three points: the FET should be fast enough to respond to the bit pulses; the total resistance and total shunt capacitance

should be low while conducting; and the voltage drop across the diode should be low. BS170 [13] and BAT85 [17] are chosen. BS170 has maximum turn-on and turn-off times at 10 ns, which is short enough compared to the expected minimal pulse width of 125 ns. Its drain-source ON-resistance $R_{DS(on)}$ is 5Ω. BAT85 has a forward voltage of 0.32V, which is small compared to the RF peak-peak voltage of 7.72V.

7.5.1 Synchronous modulation

If the 'Bitout' port outputs a binary '1', its timing position and pulse width are the same as the Hybrid_CLK cycle No.7. Its falling edge then triggers a mono-stable, generating a pulse whose duration is between 250 ns and 375 ns. This pulse is fed to the FET gate, and keeps it conducting between $t_1 \sim t_4$. However, due to the diode, the current flows only when the RF is on the positive cycle. Therefore, it is equivalent to the switch conducting between $t_2 \sim t_3$. Using the diode also allows wider tolerance on the pulse width: the position of t_4 can be from t_3 to $t_3 + 125$ ns.

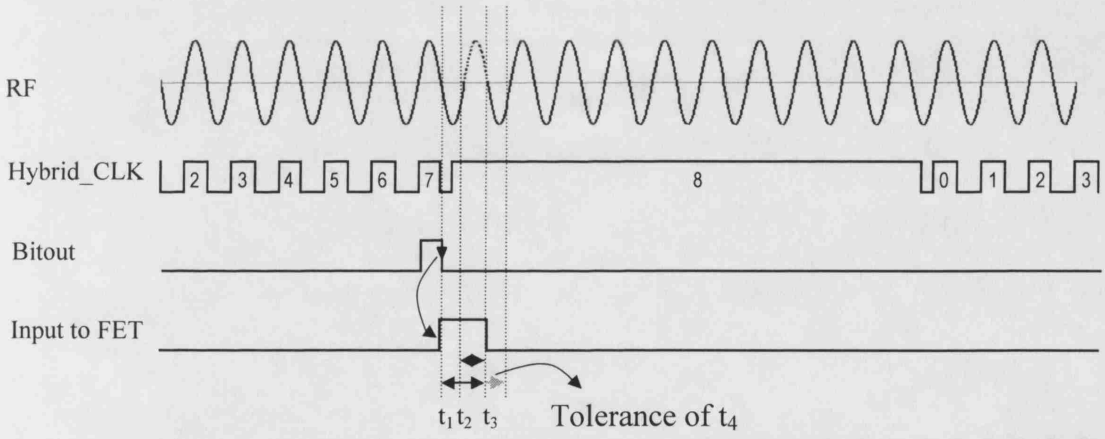


Fig. 7.13 Timing diagram for the synchronised modulation

7.5.2 Implementing the implant circuit

The schematic diagram of the implant circuit is shown in Appendix 8. The circuit has a few discreet components, 4 commercial ICs and a CPLD. The logic function is programmed into a single CPLD device, including all the elements in the logic block and most elements in the clock generation circuit except Mono-stable 1. The program is written in VHDL, and synthesised in ISE WebPACK, version 6.2i (Xilinx, Inc). Physical

fitting to the target CPLD XC2C64 is via Parallel Download cable IV (Xilinx, Inc). The VHDL program and the pin out for the implant logic are in Appendix 8.

Chapter 8 PPSM system design – The external circuit

8.1 Overview

The external circuit has the following tasks (Fig. 8.1): to recover the digital bits from the modulated RF carrier (demodulation), to sample the recovered bits at the correct positions (bit synchronisation), to group the bits into words (word synchronisation), and to output the data in an analogue format (D/A conversion). The process will be discussed in this chapter.

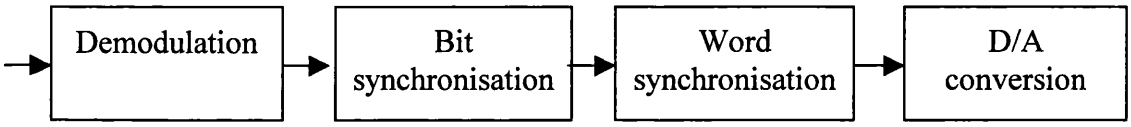


Fig. 8.1 Overview of the external circuit design.

8.2 Demodulation

Demodulation design is specified in Fig. 8.2. It consists of a voltage divider, an envelope detector, a filter, an amplifier and a level detector. A small RF voltage, which is proportional to the voltage across the tuning capacitor networks, is taken by the voltage divider. The envelope of the RF carrier contains the modulation information, which is subsequently extracted by the envelope detector. The extracted envelope is still contaminated with the unwanted carrier frequency and its harmonics. The filter eliminates them. The filter also attenuates some of the low frequencies within the signal band to reduce interference between the bits. The cleaned signals are then amplified to an appropriate amplitude level, and a level detector converts them into square pulses.

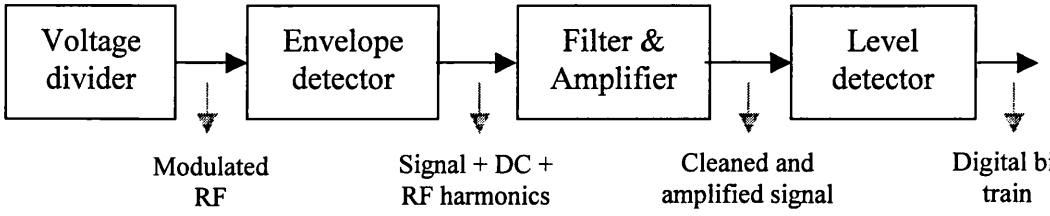


Fig. 8.2 Overview of the demodulation

8.2.1 Voltage divider

The voltage across the tuning capacitor C_1[1] or inductor L_1 in the primary circuit follows the variation in the transmitter current i_1: either can be used for demodulation (Fig. 8.3 (A)). However, using them directly has two problems. First, their amplitudes are too large. For example, in our system, v_{C1} is measured up to $300V_{p\text{-}p}$ at a coil spacing of 80mm. A large voltage amplitude requires high voltage components in the following stage. Second, connecting C_1 or L_1 directly to the following demodulation circuit makes their values easily affected by the capacitance and inductance from the next stage, so that the primary circuit could be de-tuned.

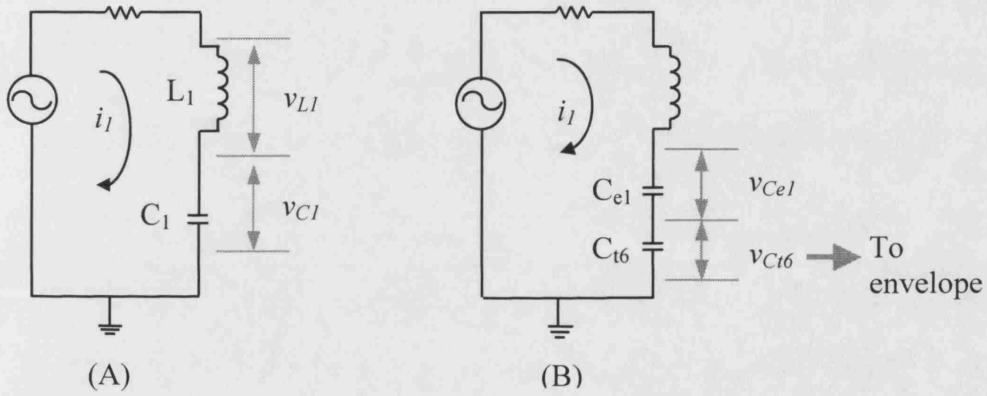


Fig. 8.3 (A): v_{L1} and v_{C1} follow transmitter current. (B): Capacitor voltage divider.

A voltage divider in Fig. 8.3 (B) is used to overcome the problems. The divider was shown in Fig 6.3, chapter 6 when discussing the transmitter circuit, except that here C_{e1} represents the total capacitance of $C_{t2} \sim C_{t5}$. The main reason for dividing v_{C1} rather than v_{L1} is that there are more choices of capacitor values to adjust the ratio.

The voltage on C_{t6} will be used for demodulation. It is expressed as $v_{Ct6} = \frac{C_{e1}}{C_{e1} + C_{t6}} v_{C1}$. Hence, in order to have a small v_{Ct6}, a large C_{t6} is required. A large C_{t6} also has two advantages: (1) the capacitance from the next stage will contribute relatively less to the variation of C_{t6}, so that the influence on the tuning of the primary

[1] A group of capacitances in the real system.

circuit is minimised; (2) a large C_{t6} gives a lower source impedance to the next demodulation stage. However, v_{Ct6} must exceed the forward voltage of the diode, which acts as rectifier in the following envelope detector circuit. So, C_{t6} should not go up indefinitely. In this system, C_{e1} is around 84 pF and C_{t6} 820 pF. The resulting v_{Ct6} ranges from 500mV to 11V when coil spacing varies from 10mm to 70mm.

8.2.2 Envelope detector

The desired signal waveform is available in the envelope of the modulated RF carrier. There are several methods for detecting an envelope: envelope detectors, rectifier detectors and synchronous detectors [94]. The envelope detector, which is constructed using a diode in series with a capacitor is simplest and is used here. Fig. 8.4 shows the circuit used in this system. C_{t6} is from the voltage divider. v_{Ct6} is the C_{t6} voltage. R is the resistance R_{e1} in parallel with the equivalent input resistance of the next stage R_{filter}. C is the capacitance of C_{e2} in parallel with the equivalent input capacitance of the next stage C_{filter}. During the positive half cycles of v_{Ct6}, when v_{Ct6} becomes greater than the sum of v_{out} and v_F (the forward voltage of the diode), D_{e1} turns on. v_{Ct6} charges C to the waveform's maximum value. As v_{Ct6} falls below the total voltage of v_{out} and v_F, the diode D_{e1} turns off, and C discharges through the resistor R until the next positive half cycle when D_{e1} turns on. The capacitor charges to the peak again and so on. Because the charge time is fast and discharge time is much slower, v_{out} only follows the v_{Ct6} envelope. The Diode D_{e2} provides a pathway to recharge C_{t6}.

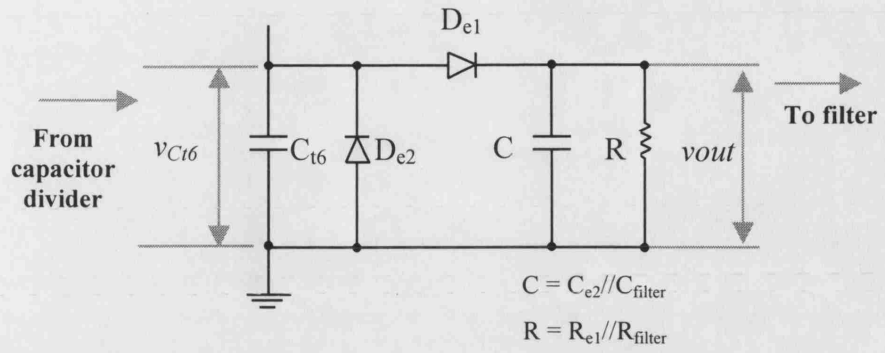


Fig. 8.4 The envelope detector.

R_{e1}: the resistance physically presented in this stage; R_{filter}: the equivalent input resistance of the next stage; C_{e2}: the capacitance physically presented in this stage; C_{filter}: the equivalent input capacitance of the next stage.

In order to extract the envelope faithfully, the discharge time constant should be optimised. If τ represents the discharge time constant, then $\tau = RC$. However, in this application, recovering the exact envelope is not important because the waveform will be reshaped by the later filter stage; and it may not even be desirable because, in the case of a beat waveform, the beats need to be eliminated at this stage. Therefore, the selection of the discharge time constant aims rather at achieving a good signal-to-interference ratio (envelope amplitude / RF ratio) and reducing the beat phenomenon.

An experiment is carried out to determine R_{e1} and C_{e2}. Connect this stage to the next filter stage. In the circuit shown in Fig. 8.4, let R_{e1} be equal to 20kΩ, C_{e2} be one of 100pF, 220pF, 320pF, 390pF, and 610pF. Let the transmitter and implant circuits work as normal. Measure v_{out} for each pair of $R_{e1}C_{e2}$. Comparing the results shows that the pair 20kΩ & 320pF produces the best signal/carrier ratio and the beats are effectively smoothed. Fig. 8.5 shows an oscillogram of v_{Ct6} and v_{out} recorded from the experiment.

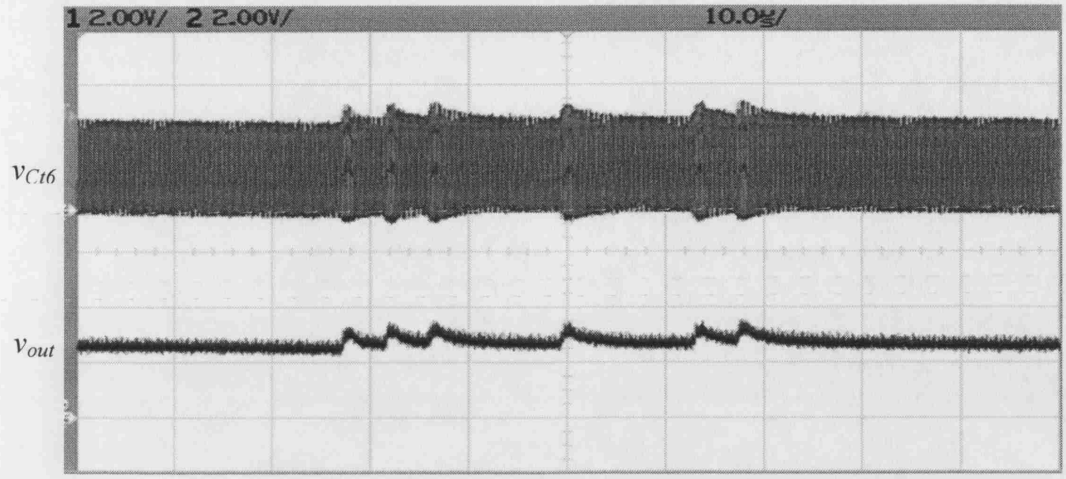


Fig. 8.5 An oscillogram showing the signals before and after the envelope detector, coil-coil spacing 36mm.

8.2.3 Filtration

The signal after the envelope detector still contains a significant amount of RF carrier frequency (4 MHz Fig. 8.6). A low pass filter is needed to clean the RF. Furthermore, the envelope shape resembles an exponential wave. It is likely to cause Inter-Symbol-Interference (ISI) [94]. That is, when two '1's are adjacent, the two modulations sometimes partly overlap due to the waveform's fall time being longer than their interval. It may generate errors when triggering the comparator (or level detector) (Fig. 8.7).

Fig. 8.6 An oscillogram showing the signal before the filter(coil spacing 36 mm).

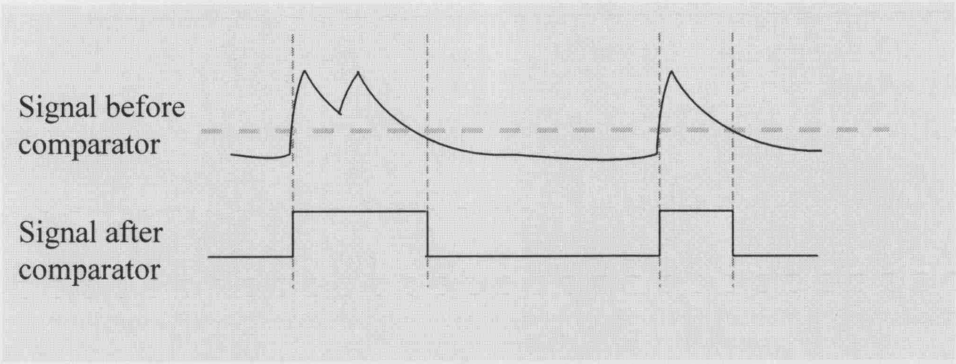


Fig. 8.7 The error caused by Inter-Symbol-Interference(ISI).

How can ISI be reduced? It can be achieved by band-pass filtration to reshape the modulation wave to an ideal waveform.

A waveform is said to be ideal if it has a uniform pulse amplitude, and sharp rising and falling edges. It has minimal chances of causing ISI, for example, a square wave. However, to shape a modulation waveform into a square wave is not easy. Instead, a waveform resembling a half-sine wave is usually regarded as doing well enough. Hence, the goal now changes to shaping an exponential-alike waveform to a half-sine wave by filtration.

Fig. 8.8 compares a half-sine wave and an exponential wave in the time and frequency domains. The exponential wave in the figure has a time constant 2.2μs, which is similar to the discharge time constant of the envelope detector. The sine function's half-period is 2μs. Compared to the frequency distribution of the exponential wave, the figure shows that the half-sine wave has a much wider band pass, extending to more than 200 kHz. The band pass of the exponential wave, on the other hand, is within 40 kHz. To shape the exponential wave to the half-sine wave, its band pass has to be widened. In order to do so, the frequencies from 10k to 300kHz in the exponential wave need to be amplified at various levels. Or, instead of amplification, band-pass filtration to attenuate the frequencies below 10k and above 300kHz can achieve a similar effect. However in either approach, the amplifier or the filter needs to be carefully designed because, for example, the amount of filtration at the different frequencies varies.

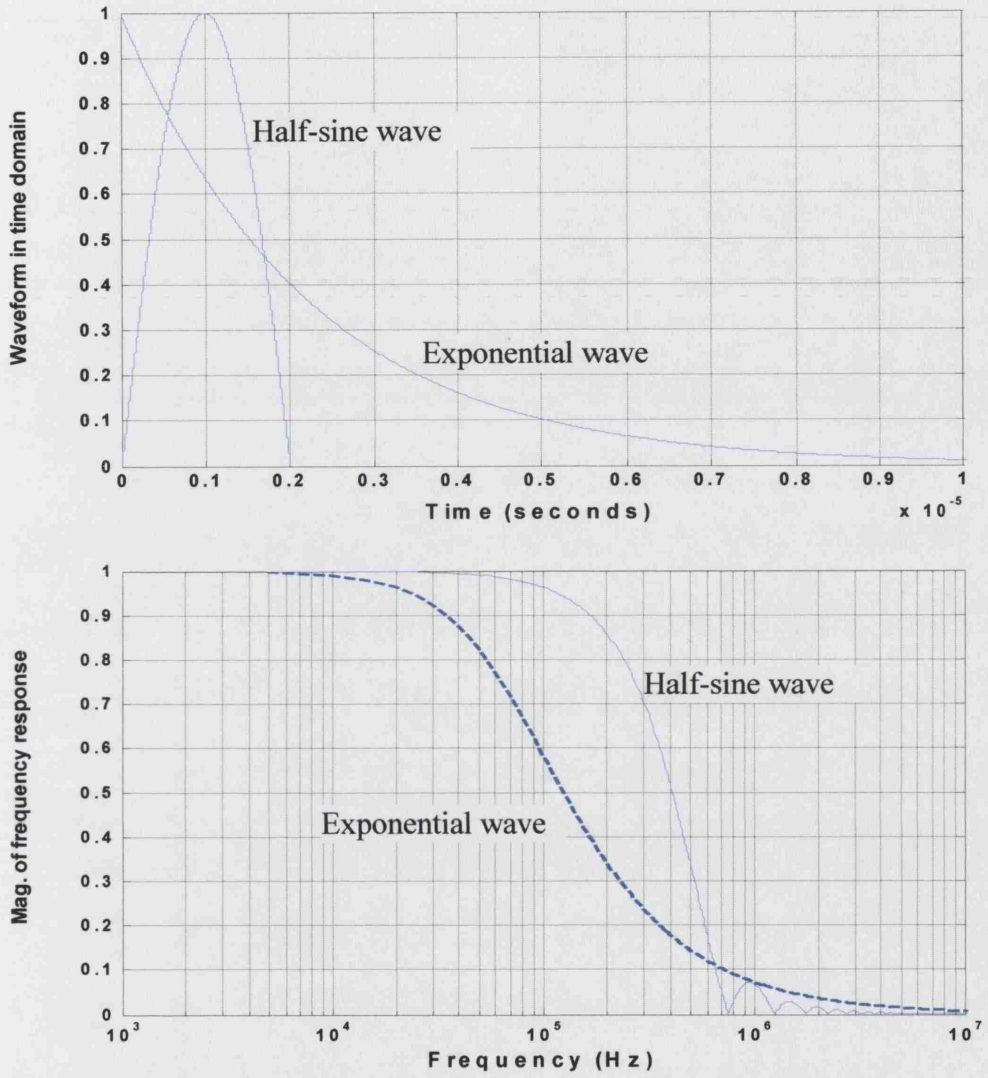
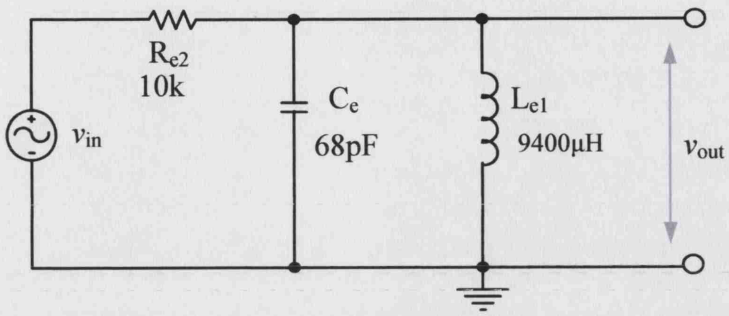
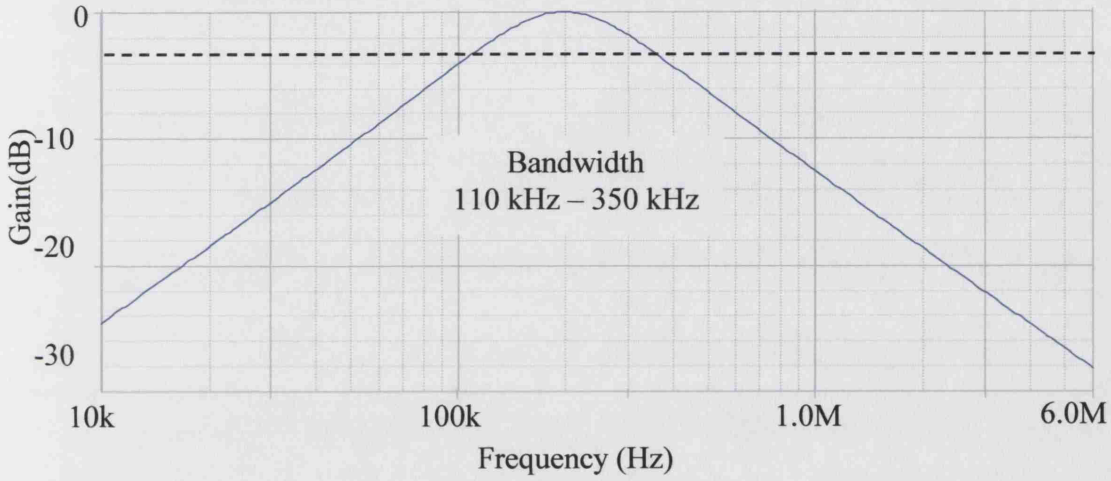


Fig. 8.8 Comparison of an exponential wave and a half-sine wave in time and frequency domains.

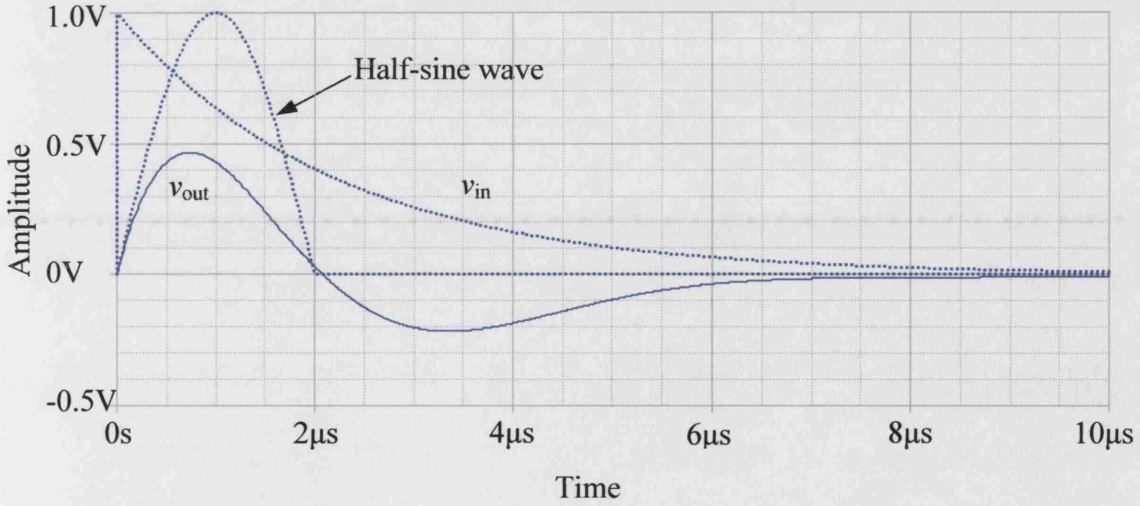
However, simulation in PSpice (OrCAD) shows that using a simple passive band pass filter yields a sufficiently good result. Fig. 8.9 (A) shows the circuit diagram of the filter, and Fig. 8.9 (B) is its characteristic which has a bandwidth 110 kHz ~ 350 kHz. Fig. 8.9 (C) plots the waveform before and after the filter (v_{in} and v_{out}). It also plots an ideal half-sine wave as a comparison. Fig. 8.9 (C) shows that the fall time of v_{out} is much reduced after filtration. Although the filtration also results in a negative overshot, it will not be our concern. Fig. 8.10 illustrates a waveform recorded from the oscilloscope after being filtered.



(A) The band-pass filter.



(B) The filter bandwidth.



(C) Comparison of v_{in} and v_{out}; and comparison of v_{out} and the half-sine wave.

Fig. 8.9 The passive band-pass filter for reshaping the signal waveform.

Fig. 8.10 An oscillogram showing an example of the signals before and after the filter, (coil spacing 36 mm).

8.2.4 Amplification

This stage is to amplify the signal to a level that can drive a comparator to generate square waveforms. Because the input to the amplifier covers a wide range (peak-to-peak value 0.1 ~ 1V), the amplifier gain is designed to switch among three levels: ×4, ×6 and × 20 when the coil spacing is 10mm ~ 40mm, 30 ~60mm and 60 ~70mm respectively. By such an arrangement, the amplifier output will be from 2 to 4V.

As the signal passband is estimated 0 ~ 200 kHz, the amplifier is required to have gain-bandwidth product of at least 4 MHz (equals 200 kHz × 20). For a portable device, the amplifier's power consumption should also be low. Several Op Amps are considered, listed in Table 8.1. LM6132 [18] is chosen as it has the lowest supply current and allows a wide range of the operating voltage.

Table 8.1 Comparison of the amplifiers

Amplifier	Maker	GBW product (MHz)	Current (mA/channel) at 5V	Voltage (V)
LM6132/6134	National Semiconductor	10	0.36	2.7 ~ 24
LM6142	National Semiconductor	17	0.65	1.8 ~24
LMH 6646/6645/6647	National Semiconductor	55	0.65	2.5 ~12
LMV721/722	National Semiconductor	10	0.93	2.2 ~5.5
LM6154/LM6152	National Semiconductor	75	1.40	2.7 ~24

The circuit diagram for the amplification is shown in Fig. 8.11. It is configured as a single supply non-inverting AC amplifier ([69] page 425). The input signal is AC coupled to the non-inverting input via C_{e4}. R_{e3} and R_{e4} form a voltage divider which biases the non-inverting input at ½ Vecc1. R_{e5} is connected to the ground via C_{e5} so that the circuit functions as a buffer for DC voltage. The output is centered at ½ Vecc1.

The output is [69]

$$V_{out} = V_{in}\frac{R_{e5} + R_{e6}}{R_{e5}} + \frac{V_{ecc1}}{2}$$

Letting $R_{e3}//R_{e4} >> R_{e5}$, $C_{e4} = C_{e5}$, the low cut-off frequency is set by R_{e5} and C_{e5}, which is

$$f_{cutoff} = \frac{1}{2\pi R_{e5} C_{e5}}$$

So, let $R_{e3} = R_{e4} = 1$ MΩ; $R_{e5} = 10$ kΩ; $R_{e6} = 30$ kΩ, 50 kΩ, or 190 kΩ; $C_{e4} = C_{e5}$ = 100 nF. The AC gain is 4, 6 or 20. The low cut-off frequency is 159 Hz.

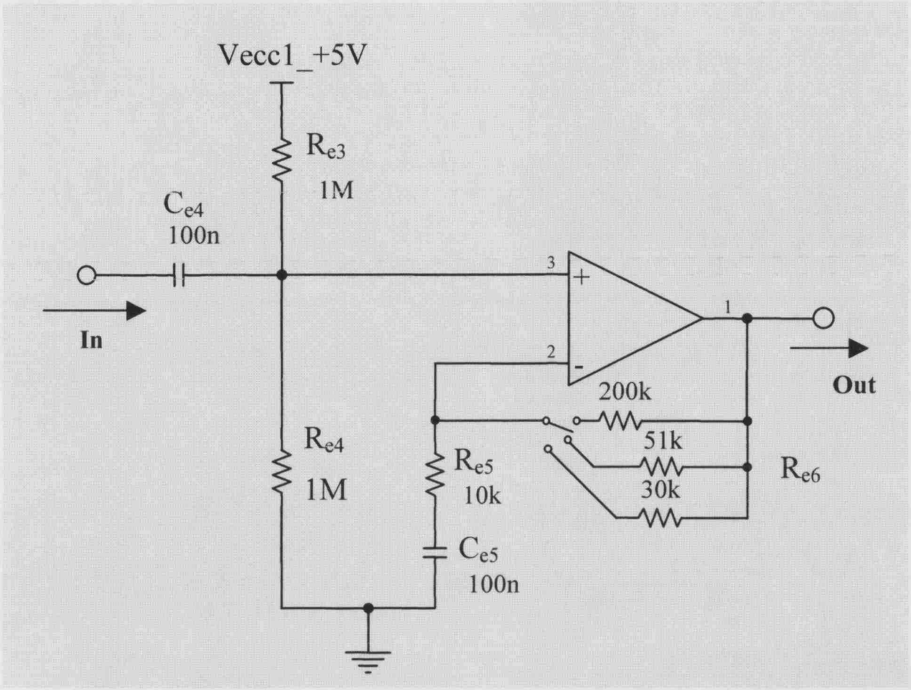


Fig. 8.11 Circuit diagram of the amplification stage.

Fig. 8.12 An oscillogram showing an example of the signals before and after the amplifier, (coil spacing 36mm).

8.2.5 Level detector

The final stage of demodulation is the level detector, or the comparator, to generate square waves.

Two comparators, listed in Table 8.2, are tested. AD8561 from Analog Devices has a propagation delay of only 8 ns, but is found to be too sensitive as it not only responses to the signal but also to the noise and the RF interference. MAX975 [16], on the other hand, performs well. Its slower speed effectively rejects the high frequency interference and is still fast enough to respond to the desired signal (a few μs pulse width). It also features very low power consumption. Therefore, MAX975 is used as the comparator in this system.

Table 8.2 Comparison of the comparators

Comparator	Maker	Propagation delay	Supply current	Supply voltage (V)
AD8561	Analog Devices	8 ns	2.2 mA	3 ~10
MAX975	Maxim Integrated Products	Low to high 0.82 μs High to low 0.48 μs	3 μA	2.7 ~ 5.25

The circuit diagram of the level detector is shown in Fig. 8.13. The input signal is AC coupled to the non-inverting input via C_{e6}. R_{e7} and R_{e8} set the DC level of the input at ½ Vecc1. R_{e9} and R_{e10} set the comparing level, in which R_{e9} is a variable resistor, adjusting the voltage from 0.45×Vecc1 to Vecc1.

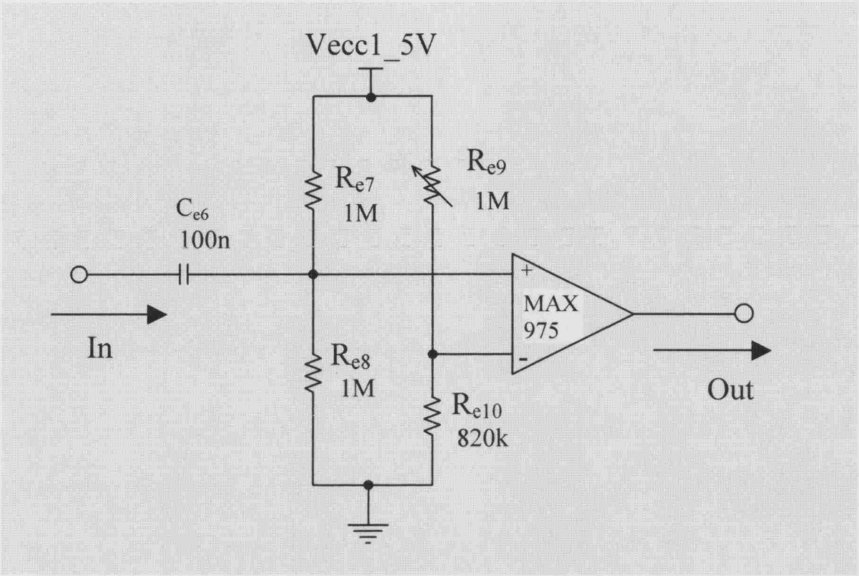


Fig. 8.13 Circuit diagram of the level detector.

Fig. 8.14 Oscillogram showing an example of the signals before and after the comparator.

8.3 Bit synchronisation

8.3.1 Introduction

The serial data pulses come out of the comparator as a stream of '1's and '0's. The next step is to read them into a buffer for processing. It requires sampling the bit stream once per bit period. A local clock oscillating at the bit rate can perform the sampling, but it must align with the incoming bit stream in order to sample them at the right instant. However, as the arrival time of the first incoming bit is random, the local clock and incoming data are usually not in a synchronised state to start with. Furthermore, after passing through the transmission channel and the demodulation procedures, the bit intervals are no longer exactly uniform. It is likely that even if they were aligned at the beginning, the bit position would drift away some time later if the local clock has a rigid, fixed frequency. Therefore, the main task of the bit synchronisation is to align the clock with the bit stream and maintain the alignment thereafter.

Bit synchronisation can be implemented by Phase-Locked Loop (PLL). PLL usually contains a phase comparator, a loop-filter and an oscillator which generates the local clock. It continuously compares the phase of the local clock with that of the incoming data. If they do not align, the oscillator's frequency will be adjusted according to the phase deviation. Hence, the clock is pulled or pushed towards the synchronised position.

8.3.2 Circuit configuration

In this design, the author uses CD74HC297 [14], an all-digital Phase-Locked Loop from Texas Instruments. Two extra components, including a monostable multivibrator and a divide-by-N counter, are needed to construct the bit synchronisation circuit.

Fig. 8.15 shows the circuit configuration. It consists of a mono-stable, a phase detector, a K-counter, a digital controlled oscillator (DCO) and a divide-by-N counter. Four inputs are required: a data stream, a K-clock to the K-counter, an I/D-clock (I/D stands for Increase/Decrease) to the DCO, and a feedback from the PLL output to the

phase comparator. Before input to the phase comparator, the pulse width of the data bit is stretched to 2.25μs (1/2 data bit period) by the monostable multivibrator. There is one output: the local clock.

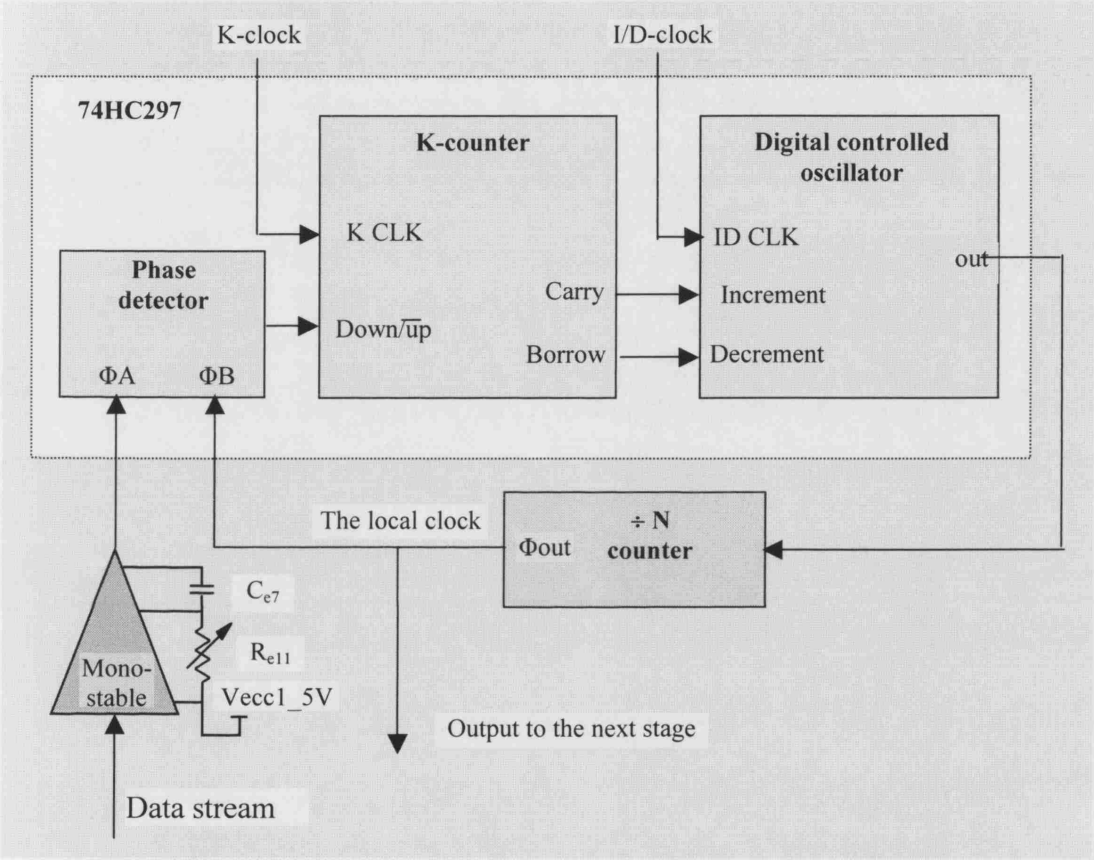


Fig. 8.15 Block diagram of the bit synchronisation.

8.3.3 Working principle

The phase comparator is an exclusive-OR (EXOR) gate. It compares the phase of the incoming signal with that of the local clock. When the data are a stream of logic '1's with a stable frequency and align ¼ data bit cycle behind the local clock, there is a zero phase error, indicating the synchronised state. The EXOR output is high for a ¼ data bit period, followed by a ¼ data bit period low (Fig. 8.16).

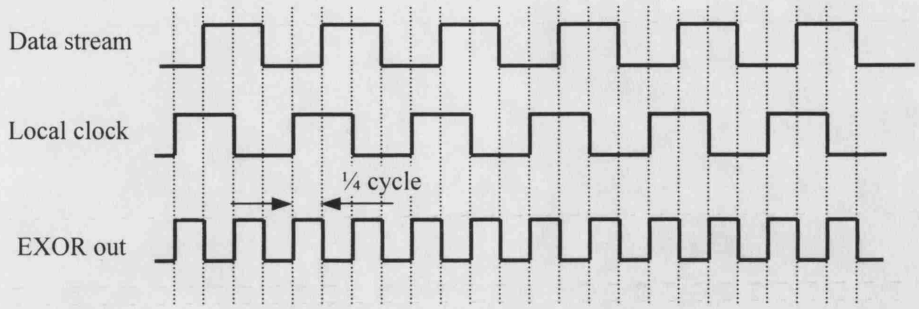


Fig. 8.16 Date and clock have zero phase error.

The EXOR output is connected to the $Down/\overline{up}$ input to the K-counter. The K-counter consists of an up-counter and a down-counter. When $Down/\overline{up}$ is low, the up-counter counts up, and the down-counter is inactive. If it is high, the down-counter counts down, and the up-counter freezes. Both counters count at the falling edge of the K-clock, and recycle to 0 when the counts exceed K-1 (Fig. 8.17). K is called the modulo of the K-counter. It is usually pre-programmed to a preferred value. For this system, the preferred value is K = 18. The reason is given as following.

The frequency of the K-clock is chosen as 16 MHz, (4 × 18) times the bit frequency f_b (222.2 kHz). Therefore, every ¼ bit period covers 18 K-clocks. In a synchronised situation like that in Fig. 8.17, the down-counter counts the first 18 K-clocks, generating a borrow pulse; the up-counter then counts the next 18 K-clocks, generating a carry pulse. Within a bit period, there are two pairs of borrow and carry pulses.

The carry and borrow signals are fed to the increment and decrement inputs of the Digital-Controlled-Oscillator (DCO) respectively. The DCO senses their rising edges, thus the duration is not of concern. The frequency of the I/D-clock is (2×36) times the bit frequency f_b. The DCO can be regarded as a divide-by-2 counter but under the influence of two control signals. In the absence of the carry and borrow pulses, the frequency of the DCO output (I/Dout) is half of the I/D-clock frequency or 36 times f_b, and an I/Dout pulse appears on every second I/D-clock. If a carry pulse is detected, an

I/Dout pulse is moved forward by one I/D-clock period. If there is a borrow pulse, an I/Dout pulse is delayed by one I/D-clock period (see Fig. 8.17, I/Dout signal).

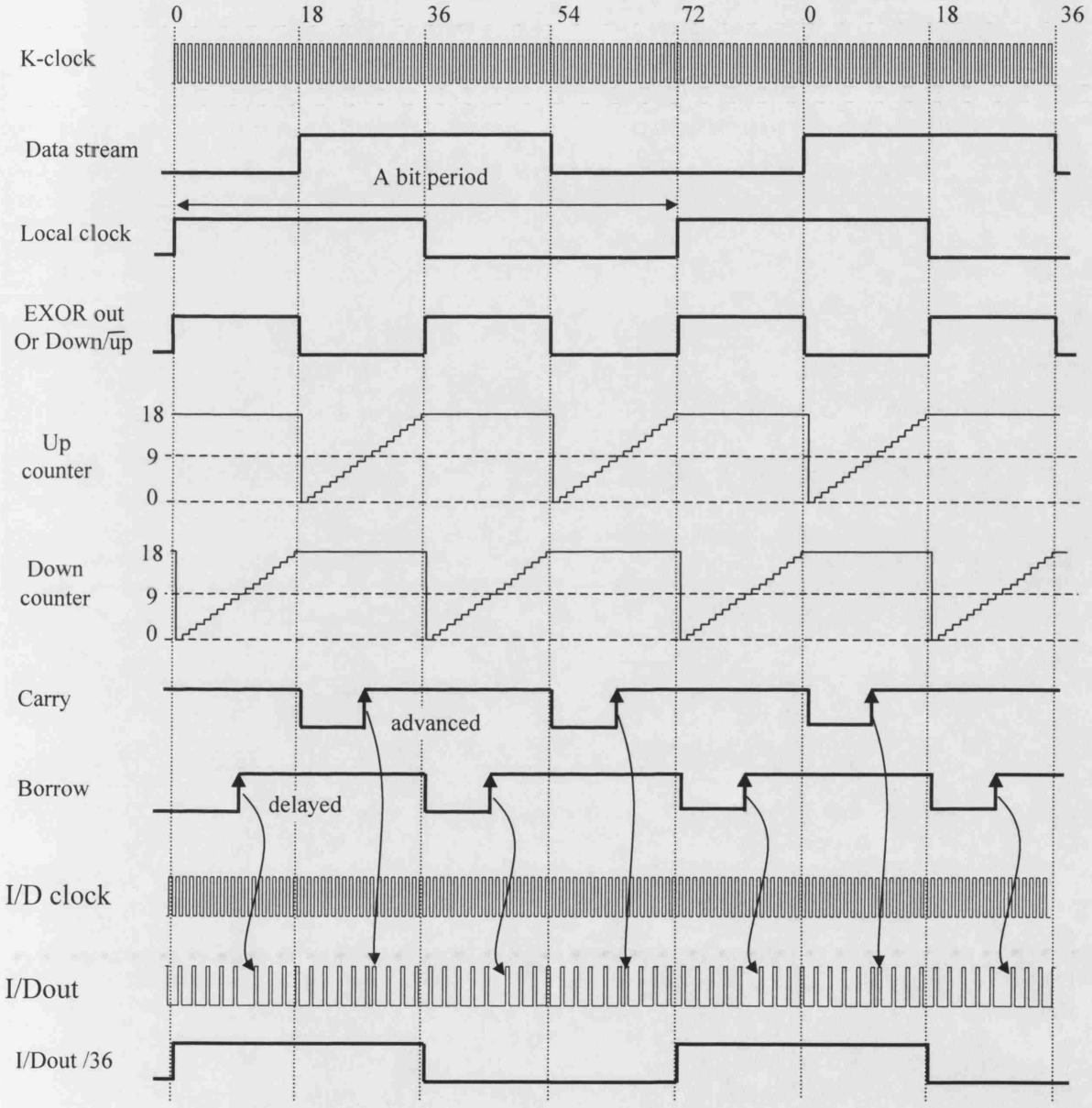
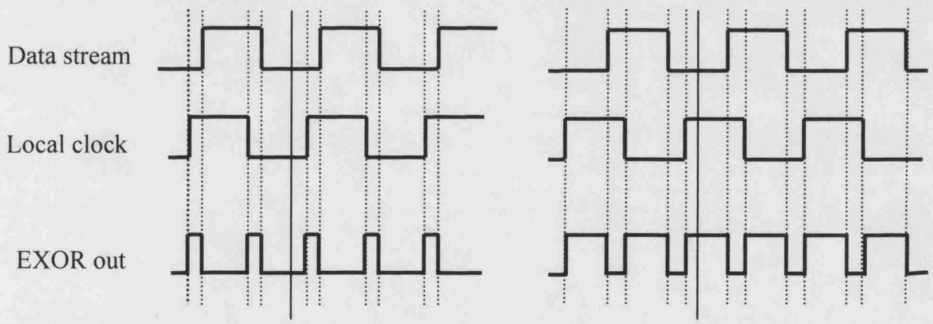


Fig. 8.17 Waveforms in the bit synchronisation. Modified from [3].

In a synchronised state, for every ½ bit period, the I/Dout pulses are moved backwards once and then forwards once, and the delayed and advanced times cancel each other out. After passing through the divide-by-N counter (N = 36), the bit frequency f_b is recovered, having a 50% duty cycle.

If there is a phase error between the data stream and the local clock, the duty cycle of the $Down/\overline{up}$ signal (or the EXOR out) becomes asymmetric (Fig. 8.18). When the clock lags behind the zero phase error position (Fig. 8.18 A), the up counter gets more clock pulses on average than the down counter. Therefore, more carry signals are generated, resulting in the I/Dout pulses being pulled forward more often than being delayed. After passing the divide-by-N counter, the local clock has shorter periods, which effectively pull the clock position forward. Similarly, when the clock is ahead (Fig. 8.18 B), more borrow signals are generated, resulting in the I/Dout pulses being delayed more often. Hence, the local clock has longer periods, which is equivalent to the clock position being pushed away.



(A) The clock lags behind (B) The clock is ahead

Fig. 8.18 Two unsynchronised situations.

Usually, a data stream is not made of all '1's. When a '0' is in the place of the bit position, no transition is observed. However, the I/D clock is still fed to the DCO, so the local clock is continuously generated. But in this situation, the phase of the incoming signal cannot be compared to the phase of the local clock, and the output of the phase

comparator (or $Down/\overline{up}$) is simply the local clock. This means the pulse width of the $Down/\overline{up}$ signal is about twice the duration of 18 K-clocks. Therefore, the K-counter will produce repeated borrows or repeated carries. Borrows and carries no longer cancel each other in ½ a bit period. This will result in an asymmetric duty cycle called jitter in the local clock. The jitter pattern is periodical when there is a long silent period caused by a long sequence of '0's [3]. In other words, the clock runs on its own pattern.

As the clock cannot be synchronised during the long silent period, it might run out of sync and sample the incoming bits at the wrong position. The factors contributing to the out-of-sync situation come from both the clock and data sides: the asymmetric clock might be out-of-phase or the data periods might not be uniform. The theoretical analysis of such situations has not been given by the available references [14], [15] and [3]. But an obvious way to reduce the out-of-sync situation is to encode the data so to avoid the very long sequences of '0's. Therefore, as discussed in chapter 7, even parity check is used for coding the bits in this design. In case all the 20 data bits from both channels are '0's, they will be followed by two '1's.

8.3.4 Design

The design is mainly selecting proper frequencies for the K-clock ($f_{K\text{-clock}}$) and the I/D-clock ($f_{I/D\text{-clock}}$), and the K-counter modulo (K). Let $f_{K\text{-clock}} = M \times f_b$ and $f_{I/D\text{-clock}} = 2 \times N \times f_b$ (f_b is the bit rate), the problem of selecting the frequencies becomes the problem of finding M, N and K. Usually, the K-clock and I/D-clock use the same clock source for simplicity, so there is

$$M = 2N$$

To have minimum jitter when in a synchronous state, we want exactly one carry or borrow generated in every ¼ a bit period. This implies that there should be K number of K-clocks during this period, or $K / (M \times f_b) = 1 / (4 \times f_b)$, gives

$$K = M/4$$

We want the bit rate f_b = 4 MHz/18 ≈ 222.2 kbit/s. Considering the above two relations, the available frequencies of the crystal oscillator, and the speed limit of CD74HC297, the author lets M = 72, N = 36, and K = 18, resulting in 16 MHz for $f_{K\text{-clock}}$ or

$f_{I/D\text{-clock}}$. However, in CD74HC297 the modulo K is set by four external programmable pins, therefore can only be 2^3, 2^4 etc. Because the optimal modulo K of 18 is not available, K = 32 is chosen instead. Such an arrangement means Up-counter or Down-counter within K-counter (see Fig. 8.15, Fig. 8.17) will generate a carry or a borrow signal when K reaches 32. Because $f_{K\text{-clock}}$ is still 16 MHz, every ¼ a bit period will have

$\frac{\frac{1}{4\times f_b}}{32\times\frac{1}{f_{K-clock}}} = \frac{18}{32}$ carriers or borrows. There are non integral number of borrows and carries in a bit cycle. In theory jitters are introduced. However, the input bits in a real system are unlikely to be all zeros or all ones for a long period; and bit duty cycle is unlikely to be a perfect 50%. In other words, jitters are part of the bit synchronisation mechanism. Observing the bench system, it works on K = 32. But in future the author would prefer to design a new DPLL chip that is similar to CD74HC297 but with K controlled by software, so K could be programmed to any desired value. This can be achieved by writing a VHDL program and implementing into a CPLD.

8.4 Word synchronisation

8.4.1 Introduction

The next step is to group bits into words. The strategy consists of an encoding and decoding procedure. The encoding was discussed in Chapter 7. It simply calculates an even parity bit for each sample, and appends it behind the data bits. Twenty data bits from the two channels and two parity bits make a 22-bits frame. They are sent out serially. The decoding for retrieving the frame from the data stream (word synchronisation) will be discussed next.

There are two inputs to the decoding stage: the data stream and the synchronised clock. They come from the bit synchronisation stage where the pulse width of the data

stream has been stretched to 2.25μs by the monostable multivibrator. There are three outputs: two 10-bit digital buses (b_{12} ~ b_{21} and b_2 ~ b_{11}), and an A/D converter enable signal. They are connected to two 10-bit digital-to-analog converters (Fig. 8.19).

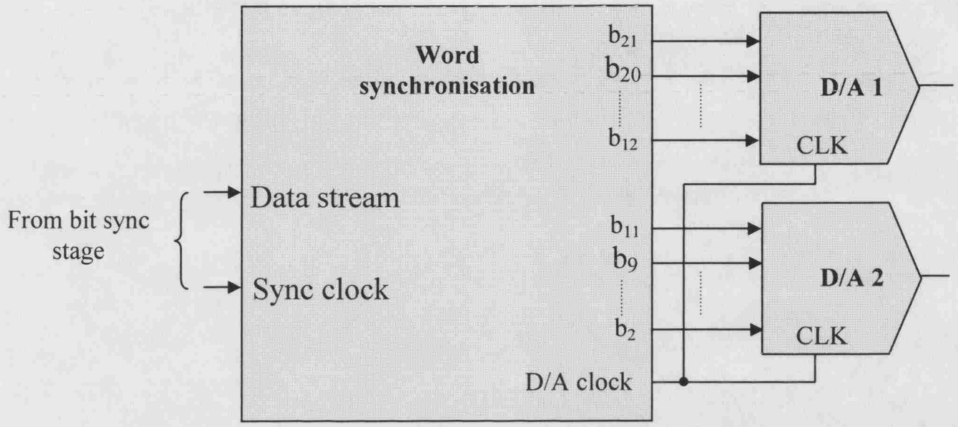


Fig. 8.19 Inputs and outputs of the word synchronisation.

8.4.2 Functional structure

A detailed block diagram is shown in Fig. 8.20.

It consists of four functional blocks: a 22-bit shift register, a parity check and comparison block, a group of 22 up-down counters and a switch for selecting a counter.

The timing diagram is shown in Fig. 8.21. CLK in the figure is the inversion of the synchronous clock from the previous stage. It is the master clock for word synchronisation.

The bits occupying the 22-bit positions in the shift register are named b_{21}, b_{20}... to b_0 from left to right. At each rising edge of the CLK, a new bit is sampled and is moved into the register. It becomes b_0. The other bits that are already in the register shift one position to the left, and the old b_{21} moves out.

The parity check & comparison block is for generating an $up/\overline{down}$ signal for the 22 counters. After a new bit moves into the shift register, b_{21} ~ b_{12} is then even parity checked by means of EXOR logic. The resulting parity bit is then compared to b_1

through another EXOR gate. At the same time, $b_{11} \sim b_2$ are being proceeded similarly and the result is compared to b_0. If both comparisons are true (or equal), the $up/\overline{down}$ signal is 'high'. If any of the two comparisons is false, it is 'low'. The 'high' indicates count up, and the 'low' means count down. This $up/\overline{down}$ is to control the 22 up-down counters.

The switch for selecting one of the 22 up-down counters is realised by a single counter. It counts one up at the CLK rising edge, and recycles to '0' after reaching 21. There are 22 control lines, named from Cnt0-en to Cnt21-en, connecting to the up-down counters respectively. They become 'high' when the switch-counter counts to a number corresponding to their names. Otherwise, they return to 'low'. Therefore, the up-down counters are selected successively.

At the CLK falling edge, the $up/\overline{down}$ signal has become stable, and the selected counter then counts up or down. If it counts up, the counter increases ***n***; and if counts down, it decreases ***m***. The number in the counter is then compared to a ***threshold***. If it higher than the ***threshold***, the 'out' signal in the counter becomes 'high'; otherwise, it is 'low' (***n***, ***m*** and ***threshold*** are integer values). The 'out' signals for the other inactive counters are 'low'. Next, all the counter outputs are ORed to give a D/A clock signal.

$b_2 \sim b_{11}$ and $b_{12} \sim b_{21}$ in the shift register are connected to $D_0 \sim D_9$ in the two D/A converters respectively. When the D/A clock is high, the data are read by the D/A converters and converted to analogue signals

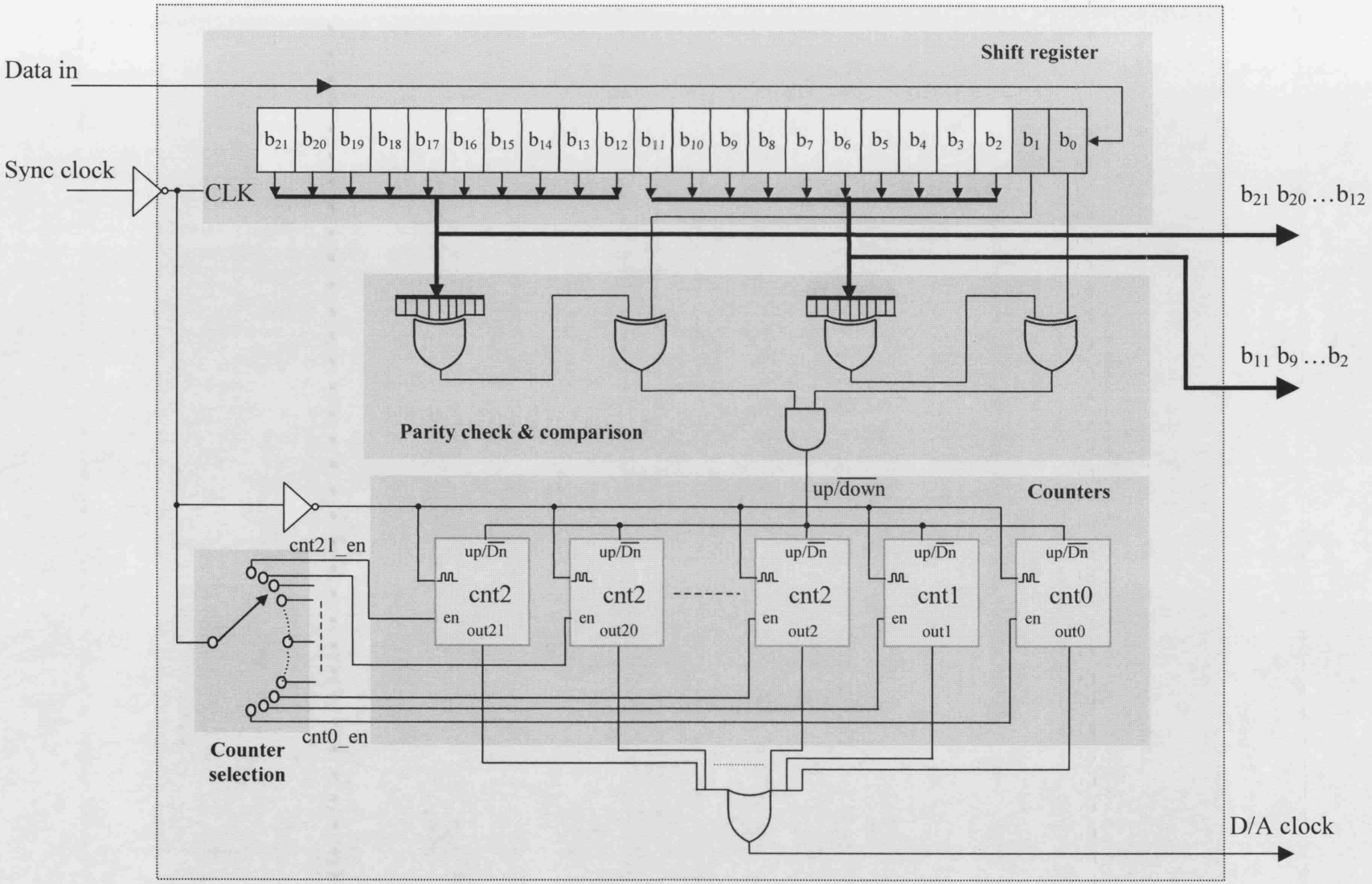


Fig. 8.20 Block diagram of the word synchronisation logic.

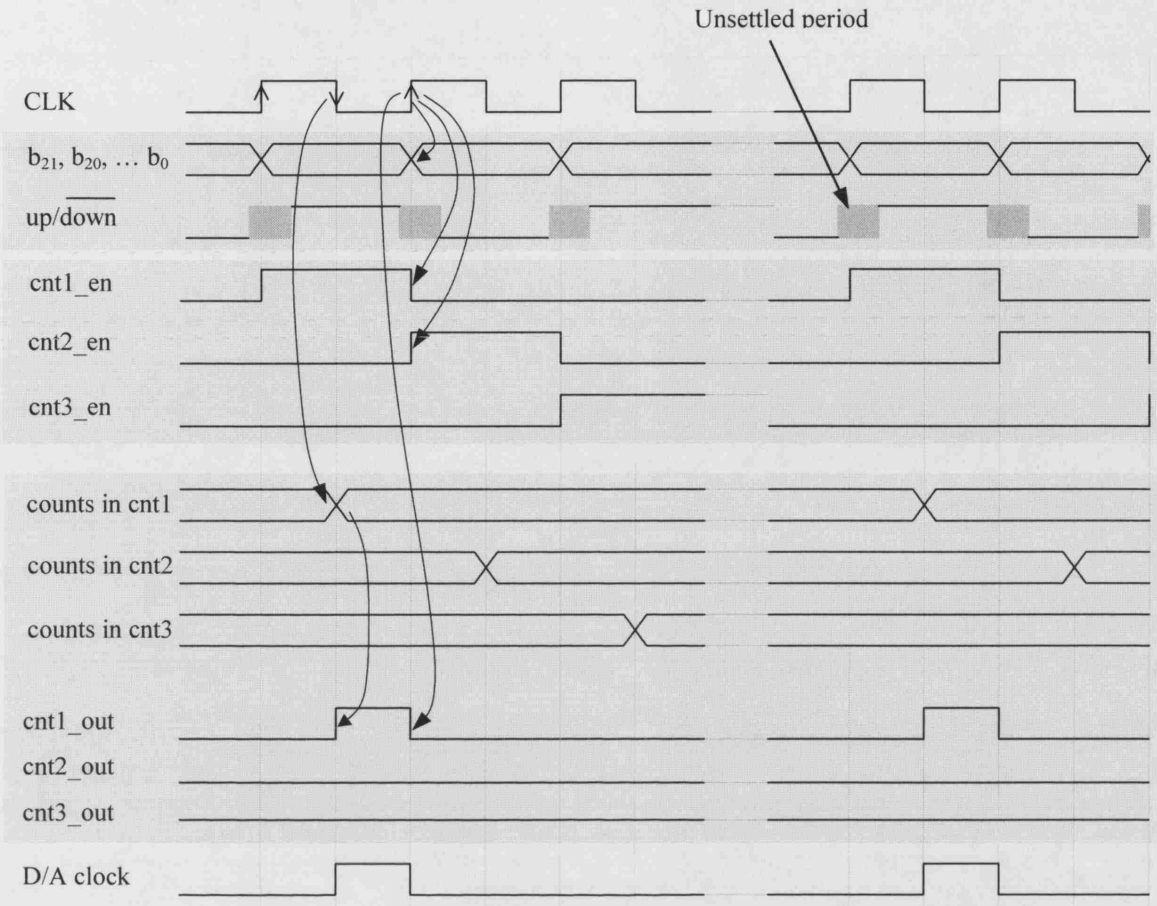


Fig. 8.21 Timing diagram of the word synchronisation logic.

8.4.3 Working principle

According to the encoding procedure, a word frame is made of 22 bits. The first 10 bits on the left make a byte for channel 1; the next 10 bits are for channel 2; and the last 2 bits are the parity bits for channel 1 and channel 2 respectively.

At the decoding side, if a whole word frame happens to occupy the 22 available bit positions in the shift register, they must have the above relations. In other words, the parity check of $b_{21} \sim b_{12}$ must be equal to b_1, and the parity check of $b_{11} \sim b_2$ must be equal to b_0. However, we need a means to detect when it will happen because the bits move in and out without obvious indications of the start and the end of the frame.

To start with, the author assumes that every time after a new bit moves in, $b_{21} \sim b_0$ represent the correct word frame. So the author tests the assumption by repeating the parity check on $b_{21} \sim b_{12}$ and $b_{11} \sim b_2$, and comparing the results to b_1 and b_0 respectively. If they are both true, the assumption might be correct, but it could also be wrong as it is possible that the combination of the data happens to give a true result. Nevertheless, we will still let the selected counter count up by '***n***' (the counters reset to '0' when starting up). On the other hand, if the assumption is tested as false, the counter counts down by '***m***', or if it is already '0', it remains at '0'.

After 22 data bits pass through the shift register, each of the 22 up-down counters has been activated once. The one which corresponds to the correct word frame definitely has '***n***'; other counters may have '***n***' or '0'. After a few hundred bits have passed through, the counts in that counter accumulate because it always counts up. The counts in the other counters cannot pass over a ***threshold*** because they count up and down randomly. The '***threshold***' is used to judge whether a counter should output a pulse or remain low. When the counter for the correct word frame is activated, its 'out' is high. When it is de-selected, its 'out' is low. For other counters, their 'out's are always low. Therefore, the pulse appears on the A/D clock line once in every 22 CLK cycles, and the A/D converters read the data accordingly.

Choosing the values for ***n***, ***m*** and ***threshold*** depends on the trade-off between reliability and the settling time (or recovery time) after an error occurs. The greater ***n*** and ***m***, and the smaller ***threshold*** allow quicker settling (or recovery) but is less reliable and vice versa. But this issue will not be pursued further in this thesis, as the main purpose of this system is to test the theory of *PPSM*. The author uses n = 2, m = 2, threshold = 12 in the design and testing on the bench shows they work well.

8.4.4 Implementation

The decoding logic is implemented by VHDL, and programmed into a CPLD XCR3384XL [24] from Xilinx, Inc. The program flow charts and the VHDL files are in Appendix 9. The programming is done at two levels (Fig. 8.22). At the bottom level, the four functional blocks in Fig. 8.20 are described in three individual VHDL files. After synthesising the files, the corresponding schematic symbols are created. At the top level,

these schematic symbols are wire-connected, producing a top level schematic file. After synthesising this top-level schematic file, it is ready for physical implementation of place and route.

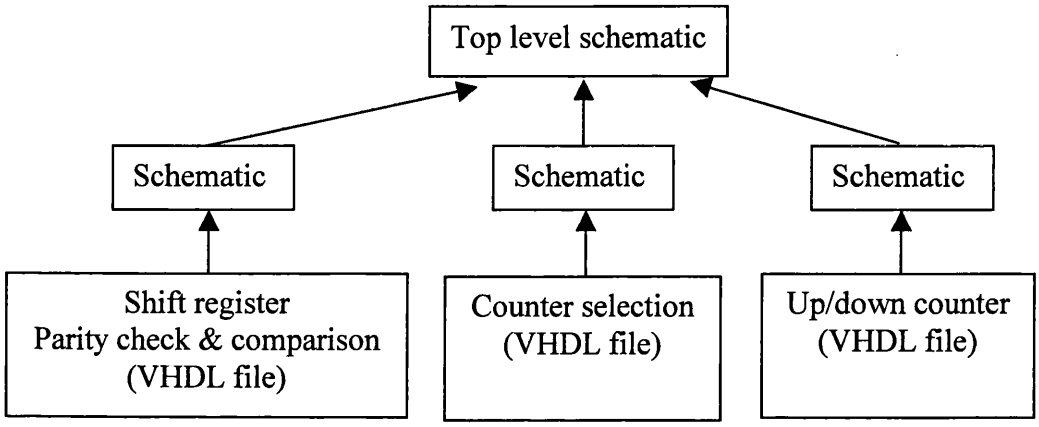


Fig. 8.22 VHDL programming structure for the word synchronisation.

8.5 D/A conversion

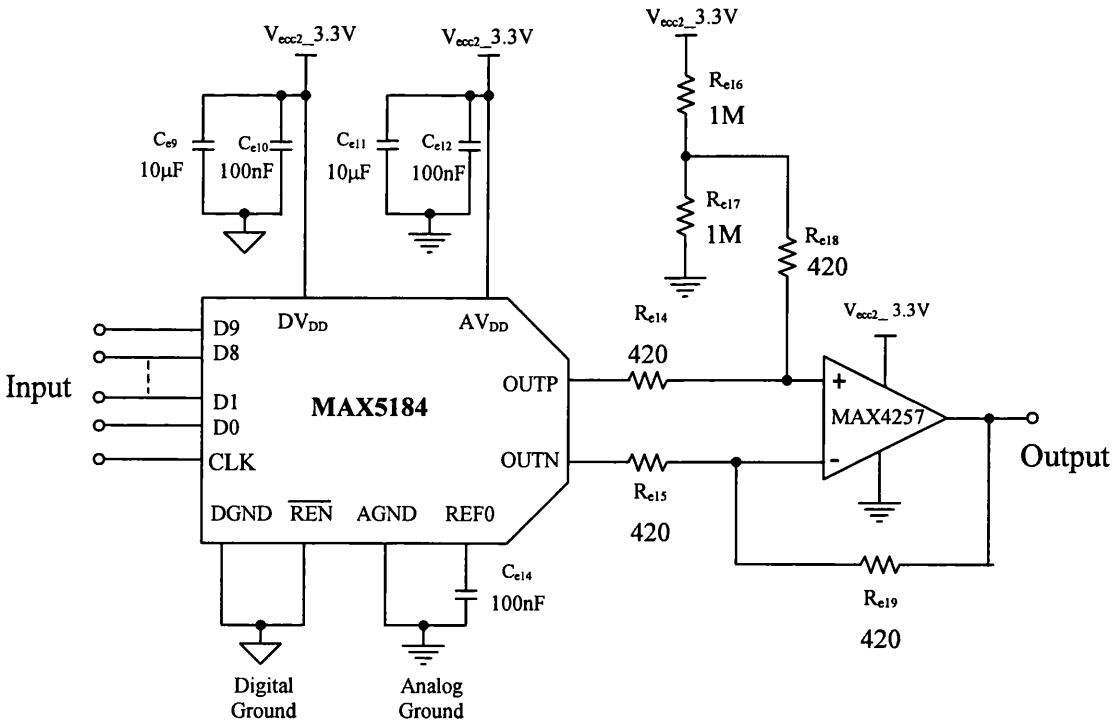


Fig. 8.23 The circuit diagram for D/A conversion.

The last step is to convert the digital signals back to analog forms. It is implemented by two 10-bit digital-to-analog converters (MAX5184 [20]) and a dual Op AMP (MAX4257 [22]) (both from Maxim Integrated Products). The Op AMP converts the differential voltages to single-ended voltages. The circuit is shown in Fig. 8.23

8.6 Summary of the external circuit

This chapter discussed the design of the external circuit. A complete schematic diagram of the external circuit is shown in Appendix 9. It consists of four main parts: the demodulation, the bit synchronisation, the word synchronisation and the D/A conversion. The demodulation recovers the modulation waveforms back to square waveforms. It includes the voltage division, the envelope detection, the filtration, the amplification, and the level detection. The demodulation circuit is constructed by discrete components and off-the-shelf ICs. The bit synchronisation aligns the sampling pulses with the bit stream. It is achieved by a digital Phase-Locked Loop. The word synchronisation reads the data bits into the internal register, and groups them according to their original word frames. The digital logic for the word synchronisation is programmed into a programmable gate array device. The D/A conversion converts the digital signals to analog signals.

Chapter 9 PPSM system design – Assessment and Test

9.1 Introduction

In this chapter, the PPSM prototype system will be assessed. The waveforms at the several stages of modulation and demodulation will be presented. The power transfer efficiencies across the inductive link when there is PPSM and when there is no PPSM are compared. The modulation waveform changes with the coil-coil distances are illustrated by oscillograms. The modulation index was measured from the system and compared with the calculated value. The theories derived from the previous chapters regarding the efficiency, waveform shape and modulation index will be assessed by the measured results.

Fig. 9.1 shows the PPSM system working on the bench.

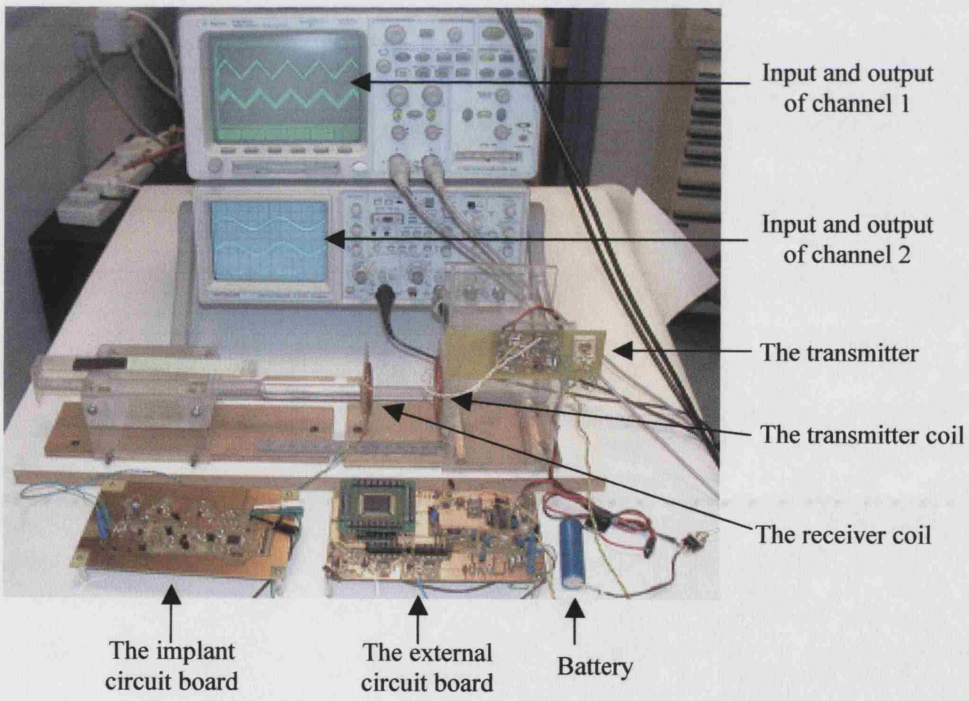


Fig. 9.1 The PPSM system

On the left side of Fig. 9.1 is the implant circuit connected to the receiver coil; on the right are the external circuit, and the transmitter driving the transmitter coil. The

coils are separated at about 70mm. A battery supplies the power for the transmitter and the external circuit. One oscilloscope displays two triangle waveforms. The upper trace is from a signal generator, and is the input signal fed to channel 1 of the A/D converter at the implant side; the second trace is the output of one D/A converter at the external side. The other oscilloscope displays two sinusoidal waveforms, which are the input and output signals for channel 2. They demonstrate that the system successfully transmits two signals via an inductively coupled power link by PPSM.

9.2 The waveforms during the modulation and demodulation

Fig. 9.2 and Fig. 9.3 are the oscillograms showing some waveforms in the implant circuit. Fig. 9.2 demonstrates 1) the RF carrier after being synchronously modulated by the data pulses, 2) Raw CLK derived from this RF and 3) Hybrid CLK; Fig. 9.3 shows the A/D interface logic.

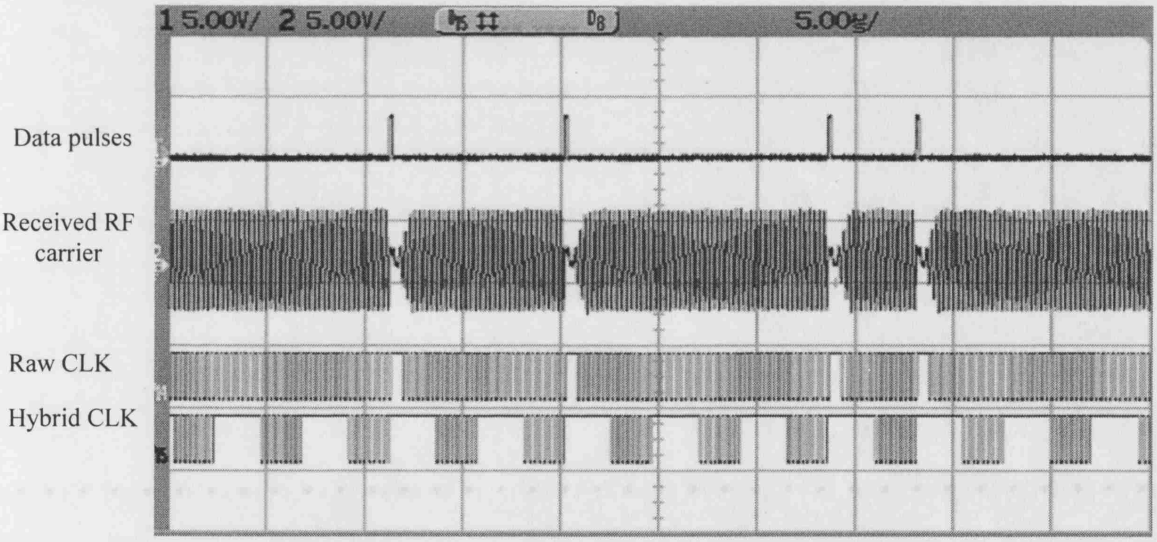


Fig. 9.2 Oscillogram of the synchronous modulation and the Hybrid_CLK generation.

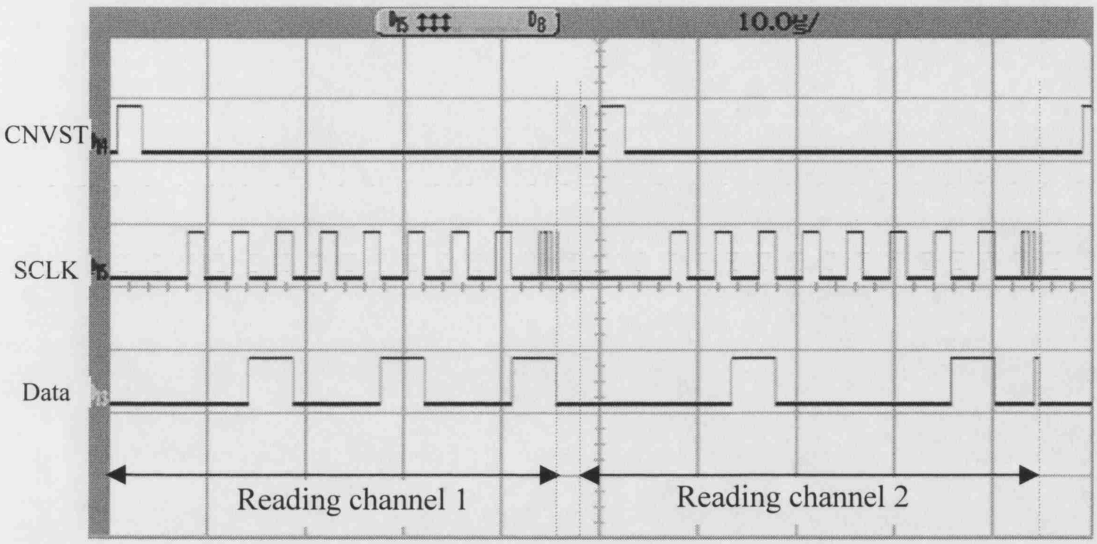


Fig. 9.3 Oscillogram of the A/D interface logic in the implant circuit.

The waveforms in demodulation stages in the external circuit were illustrated in chapter 8. They are summarised in Fig. 9.4.

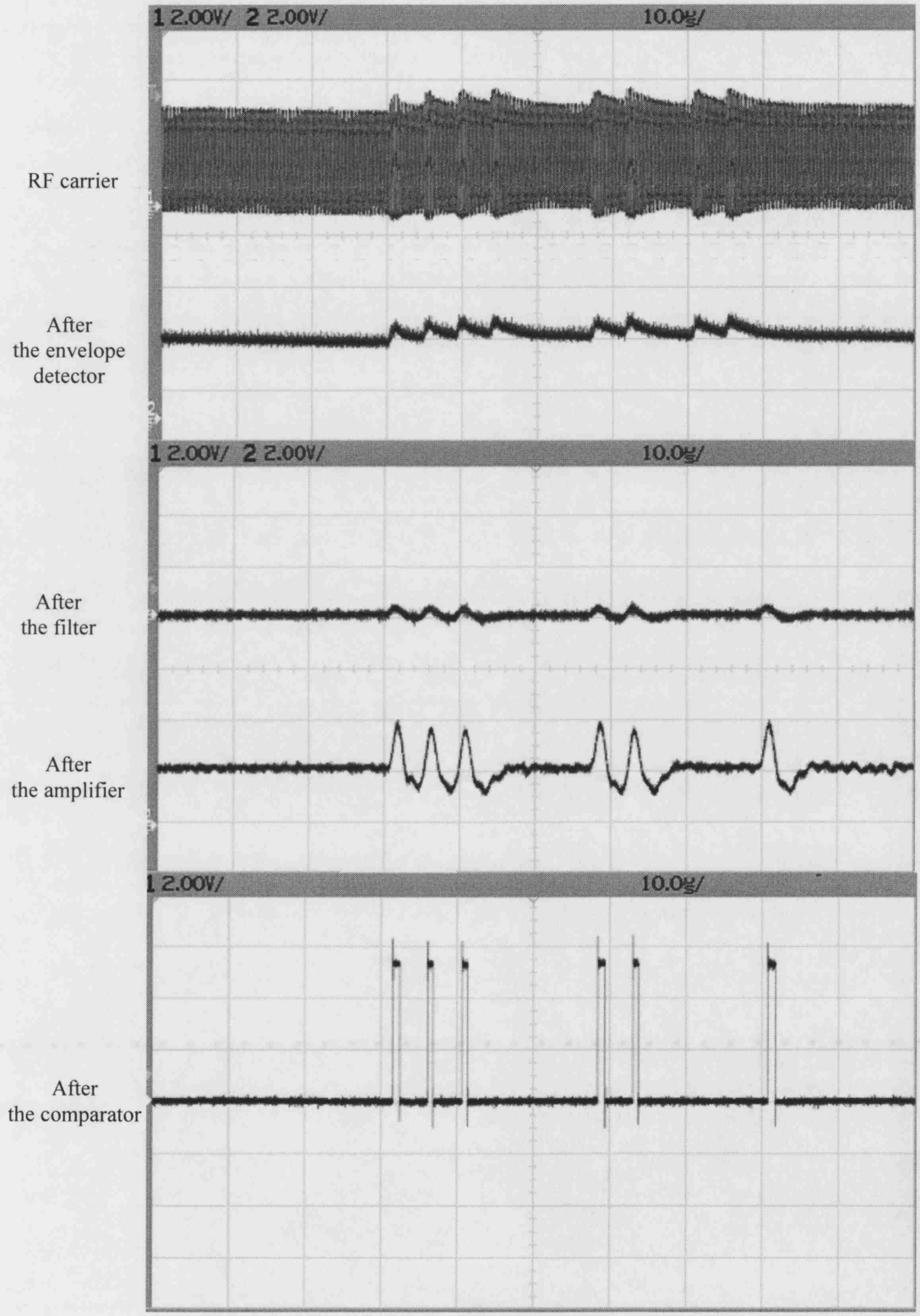


Fig. 9.4 Oscillograms of the waveforms during demodualtion in the external circuit, coil-coil spacing 36 mm.

9.3 The Power link

In this section, two measurements regarding the power link are presented: the transmitter voltage Vtcc2 required for stabilising the implant voltage at the different coil-coil distances; and the power transfer efficiencies when there is PPSM and when there is no PPSM. The aim is to verify the theoretical and simulated results described in Chapter 6 and Chapter 3.

9.3.1 Transmitter voltage Vtcc2 versus coil-coil spacing

In section 6.5, Chapter 6, a coupling compensation method for stabilising the implant voltage was described. In this method, the primary current is measured to detect the degree of the coupling (or coil-coil spacing, Eq.6.3), and the transmitter supply voltage Vtcc2 is then adjusted according to the coupling to achieve a stable implant voltage. The relation between Vtcc2 and coupling coefficient k is represented by Eq. 6.2. In this section, the theoretical Vtcc2 calculated from Eq. 6.2 when the implant RF voltage is kept at 7.2V[1] is compared with the measured result. Fig. 9.5 plots Vtcc2 versus coupling coefficient relations. The solid line is the measured curve and the dash line the theoretical result. Note that the coil-coil spacing in Eq. 6.2 is converted to coupling coefficient according to Fig. 2.4 in Chapter 2.

Fig. 9.5 shows that the measured curve basically agrees with the calculated curve except two aspects. First, the two curves are slightly displaced along k axis (Δk is about 0.002~0.005). This may be caused by the errors during the distance~k conversion. Note that it is a straightforward Vtcc2 versus k relation in the calculated curve. While in the measured curve, the relation of Vtcc2 versus coil distance was found out firstly, then the coil distance was converted to the corresponding coupling coefficient k, and Vtcc2~k curve was plotted. Inaccuracy in coil alignment, or ignorance of stray inductance and capacitance of the cables and leads all introduce errors in the distance~k conversion measurement (Fig. 2.4, Chapter 2, or Appendix 3). Hence, misplacement of $\Delta k \approx 0.002$~0.005 is expected. In fact, when implementing this coupling compensation method electronically, coupling coefficient k will be estimated from the primary current

(Eq. 6.3). There will be no need for distance~k conversion. So the displacement in Fig. 9.5 is not of great concern. Second, if we move the measured curve to the right for $\Delta k \approx 0.005$ to offset the displacement error, the measured curve is generally greater than the calculated curve regarding Vtcc2 axis. The possible reason is that the power losses in FETs are included in the measurement but not considered in calculation. Thus, the transmitter voltages are higher in a real system. It indicates that it may be necessary to verify the transmitter voltage ~ k relation experimentally when designing a coupling compensation circuit.

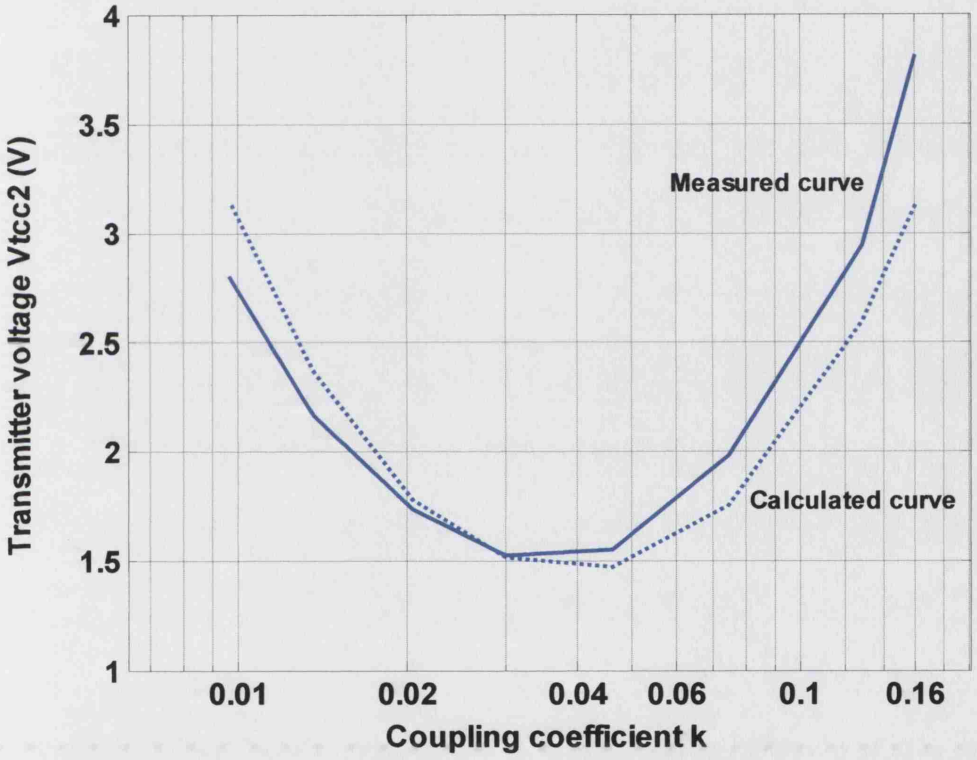


Fig. 9.5 Transmitter voltage Vtcc2 versus coupling coefficient for stabilising the implant voltage at 7.2V.

[1] Observed from the bench system, the regulator 1 output is just about 3.3V when the RF peak-to-peak voltage is 7.2V. Note that it is less than the calculated value 7.72V in Section 7.2, Chapter 7. The difference may due to variation in the component's parameters.

9.3.2 Power transfer efficiency

The aims of this section are 1) comparing the power transfer efficiency (without modulation) measured from the bench system with the calculated result by the equation derived from Chapter 2; 2) comparing the difference the modulation makes on the power transfer efficiency.

The equation for calculating power transfer efficiency is Eq.2.22, Chapter 2, and is rewritten as follows

$$\eta_{overall} = \frac{1}{1+\frac{1}{k^2 Q_1 Q_2}} \times \frac{1}{1+\frac{R_{eq}}{R_r}}$$

The power consumed by the implant electronics is given as $P_{implant}$ = the output voltage times the output current from Regulator 1 (3.3V×2.8mA). The power supplied to the transmitter is given as P_{supply} = the output voltage times the output current from the power supply to Vtcc2 (see transmitter circuit diagram in Chapter 6). At each given coil-coil distance, Vtcc2 voltage is adjusted to a level which makes the output of Regulator 1 in the implant circuit just reach 3.3V. The measured efficiency is $P_{implant}$ / P_{supply}. The calculated curve, the measured curves with and without the modulation are all plotted in Fig. 9.6.

Fig. 9.6 shows there are discrepancies between measured and predicted curves. The measured efficiency is lower than the calculated result; and unlike the calculated efficiency, it drops when the coil-coil distances are small. The reason for the first phenomenon is that the calculation considers the ideal situation only, while in an ideal situation, the power losses in the FETs, the diodes and the regulator are ignored. The cause for the second phenomenon is as follows:

In the measurement, P_{supply} includes the power losses in the FETs. Tests show that these power losses increase when the supply voltage Vtcc2 goes up. The main reason is as following: the two complementary FETs (Fig 6.3, Chapter 6) are both partially on for a brief period (about 10 ns, according to the manufacturer's data) during which one is being switched on, while the other is being switched off. It results in a brief

short-circuiting between Vtcc2 and Ground. So the higher the Vtcc2, the more the power is lost. From Fig. 9.5 we know that within 40 mm coil distance (or k > 0.05), the supply voltage goes up when the coils get closer. Hence, the power loss in the FETs increases accordingly. On the other hand, the actual power needed to supply the implant decreases when the coils get closer. This results in the power losses in the FETs becoming more and more dominant in P_{supply}, and so the efficiency drops.

Fig. 9.6 also shows when there is modulation superimposed onto the power link, the power transfer efficiency is slightly lower compared to the power transmission only situation. It agrees with the prediction in Chapter 3 where the power consumption in PPSM was analysed in simulation.

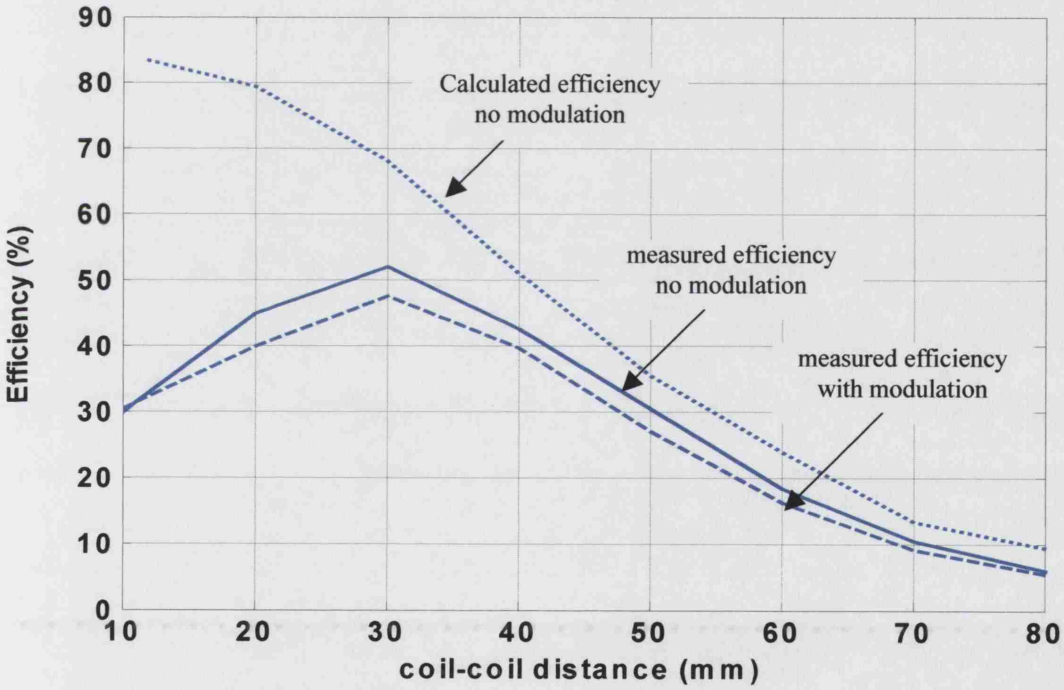


Fig. 9.6 Comparison of the power transfer efficiencies.

9.4 The data link

This section will show the modulation waveforms recorded from the bench system and the modulation index calculated from the measurement. The results will be compared to the prediction derived from the theory in Chapter 5.

9.4.1 Modulation waveforms at different coil-coil distances

The voltages on C_{t6} (see transmitter circuit diagram in Chapter 6) are recorded by an oscilloscope when the coil-coil distance is 10 mm, 20 mm, 30 mm, 40 mm, 50 mm and 60mm; and shown in Fig. 9.7. The scales in Fig. 9.7 are as follows: vertical (amplitude), 1.00V/div; horizontal (time), 2μs/div. Only part of v_{Ct6} is displayed in the 40mm, 50mm, and 60mm oscillograms.

Fig. 9.7 shows that as the coil-coil distance increases, the amplitude of the modulation waveform decreases (from 1.85V down to 200mV). From 10mm to 30mm, the waveform shows signs of beat phenomenon. The results agree with the expectation from the theory in Chapter 5.

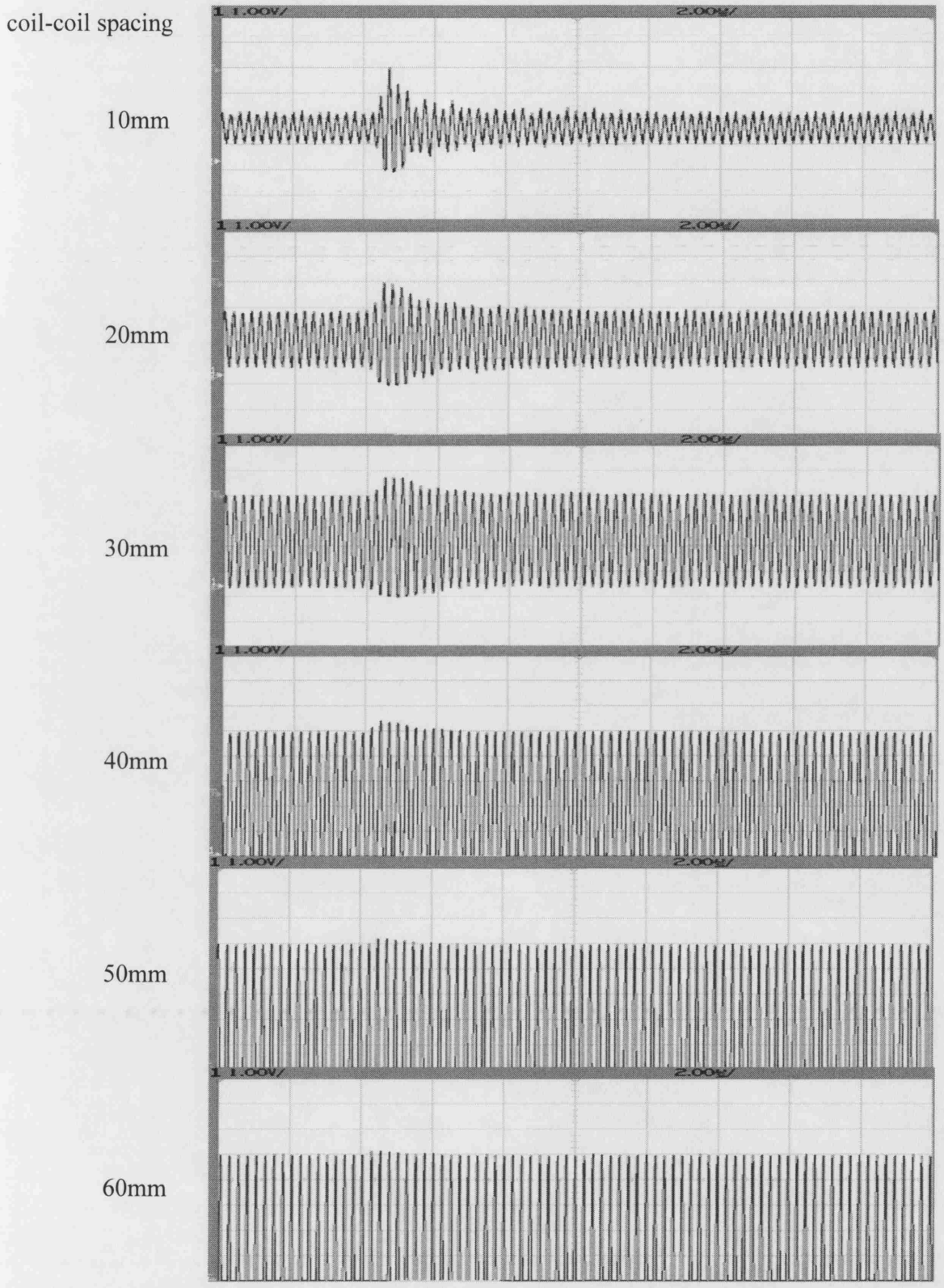


Fig. 9.7 Oscillograms of the modulation waveforms at different coil-coil distances.

k is getting greater, the measured modulation index is significantly larger than the calculated one. It can be explained as below:

To arrive at Eq. 5.3 and Eq. 5.4, we used the initial conditions Eq. 4.19~Eq. 4.22. However, as having been discussed in Section 4.4.2, Chapter 4 (or Section A.5.7.3, Section A.5.8.1, Appendix 5), one of them, namely $v_{C1}(t_0) \approx V_{C1\max}$, is only true for smaller ks. At a greater k, $v_{C1}(t_0) > V_{C1\max}$ (see Fig.A 5.7). We know that using $v_{C1}(t_0) \approx V_{C1\max}$ will give smallest modulation amplitude. The measured modulation amplitude, on the other hand, is contributed from a real $v_{C1}(t_0)$, which is greater than V_{C1max}. Hence, the results shown in Fig. 9.8 are expected.

9.5 Conclusion

This chapter demonstrated PPSM is a feasible modulation concept that is achievable practically.

Fig. 9.1 shows the system conveys a saw tooth signal of 1 kHz and a sinusoidal signal of 500 Hz across the RF link while the coils are separated at about 70mm (k = 0.014). Such coil-coil distance is close to the worst case this system is designed to work for. The carrier is 4 MHz and the data rate is 222.2 kbit/s. The bit rate/carrier ratio is 1/18. The lower traces on each oscilloscope are the recovered signals directly come from the outputs of the A/D converters. They have not been filtered, therefore noisy. The conversion of the analogue signal from the digital signal in this design is for demonstration only. In a real feedback system, the digital signal before the D/A conversion will be used for signal processing.

The digital and analogue waveforms during the modulation and demodulation processes were presented.

The required transmitter voltage Vtcc2 for stabilizing the receiver voltage, the power transfer efficiencies with or without modulation, the modulation waveforms and the modulation index were measured or recorded, and compared to the theatrical predictions. The results showed that they agree with the expectation from the theory.

9.4.2 Modulation index

At each given coil-coil distance, measure the maximum and normal steady state amplitudes of v_{Ct6}. The amplitudes are denoted as Vmax and Vsteady respectively. Calculate modulation index by $m = \frac{V\max - Vsteady}{V\max + Vsteady}$, convert the coil distance to the corresponding coupling coefficient k by Fig. 2.4 in Chapter 2, and plot m versus k curve in Fig. 9.8 (marked as Measured curve).

For comparison, the modulation index is also calculated from $i_{1natural}$ by Eq.5.25, where $i_{1natural}$ is given by Eq.5.4 (the method is described in Section 5.5.3, Chapter 5). The calculated curve is the dash line in Fig. 9.8.

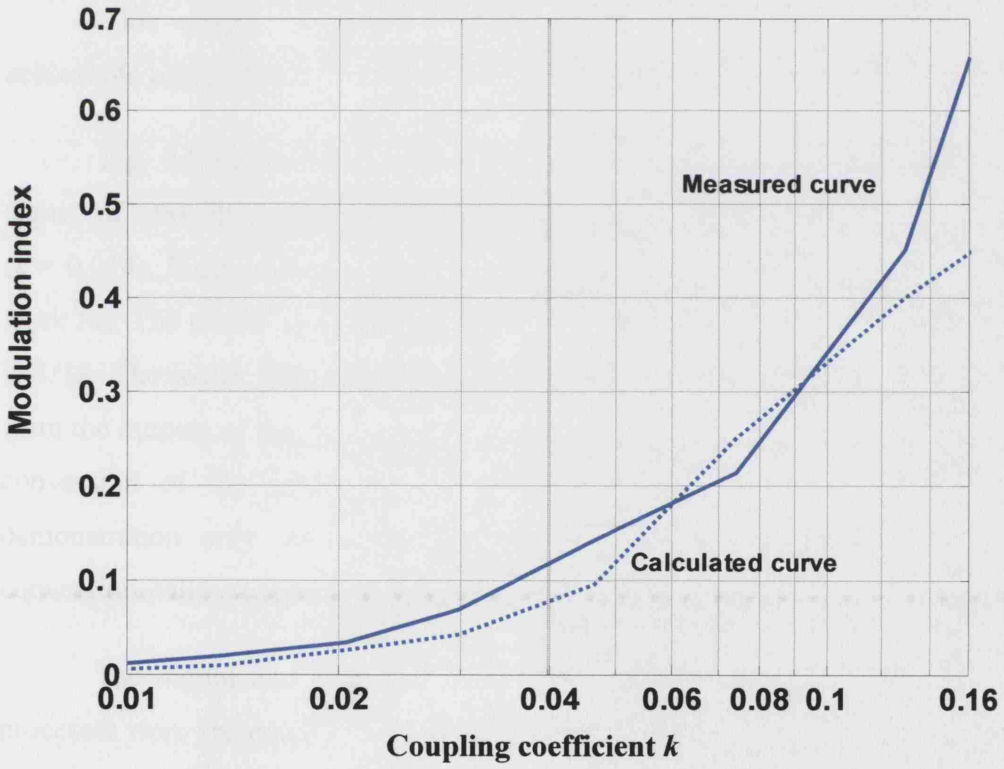


Fig. 9.8 Comparison of the modulation index.

Taking into account the errors in reading the amplitudes, and the inaccuracy in coil distance to k conversion mentioned in Section 9.3.1, Fig. 9.8 shows approximately the measurement agrees with the calculation except for the greater ks (for $k > 0.1$). When

Further measurements to test performance of the bit and word synchronisation may be needed to estimate the reliability of the digital part of the system. For example, the capture time and the error recovery time in the encoding and decoding strategy; and the jitters, lock range, error rate, etc, in the digital phased-locked loop based bit synchronisation design. However, they are not investigated further here because this thesis intends to concentrate at the new modulation concept - PPSM.

Part 4

Discussion

Chapter 10 Discussion

10.1 Summary of the research

This thesis describes a novel passive modulation method - *Passive Phase Shift Modulation* or PPSM for high-speed data transmission in feedback implantable neuroprostheses. It also presents the design and evaluation of a telemetry system which implements PPSM.

In this method, power is provided to the implant device via an inductively coupled RF link. Physiological signals are continuously conveyed out of the body via the same RF channel. Its working principle is different from that of conventional *Passive Impedance Modulation*, in which the implant impedance is modified. PPSM controls energy redistribution to generate modulation. It synchronously shorts the implant power-receiving coil for half the carrier cycle when a digital binary bit '1' is transmitted. This action holds the energy in the coil and then releases it back to the circuit in time to generate a transient current surge in the transmitting coil. Each transient surge indicates a modulation. Note that PPSM scheme transmits phase shift modulation, but results in amplitude modulation in the primary current.

The mechanism of PPSM was explored by PSpice simulation and theoretical analysis. The mathematical function of the transient waveform was derived by two approaches: 1) mathematically deducing the analytical solutions and 2) a semi-numerical method using modern computer aided tools. Formation of the waveform was thoroughly studied and influence of the circuit parameters was analysed. The waveform is made by a natural response superimposed onto the steady state response. Its characteristics are mainly determined by the natural response. The natural response, $i_{natural}$, is composed of two damped cosine functions. The properties of the two damped cosines change along the k axis, resulting in a gradual change of the modulation waveform shape. From a weaker coupling to a stronger coupling, the single peaked modulation waveform develops to the beat waveform. The modulation amplitude also increases. Its duration is determined by $1/\alpha'$. Q_1 and Q_2 also affect the modulation waveform, and the influence from Q_2 is more significant.

The electronic system for implementing PPSM was designed, built and assessed. It consists of a transmitter, an implant circuit, an external circuit and two coils. The bench system is able to convey two channel analogue signals, each having a 5 kHz bandwidth, from the implant to the external side via a pair of coupled coils by PPSM. The carrier is 4 MHz, and the data rate is 222.2 kbit/s. For both power and data transmission, the working coil-coil spacing is up to 70mm.

The above studies show that PPSM retains the good features of *Passive Impedance Modulation* by using the same RF carrier for both power and signal transmission, but achieves higher speed, better energy efficiency and simpler circuit design with comparable working range. The research also theoretically explains why the transient waveform generated by PPSM is suitable for representing a modulation within the required working ranges of k, Q_1 and Q_2; and the circuit parameters optimised for power transfer link in the author's application are good for signalling as well. In other words, the signal link does not disturb the optimised efficient power transfer link. Finally, and most important of all, the prototype system demonstrates that PPSM works practically.

10.2 Test of hypotheses

Five hypotheses were proposed in Chapter 1 and tested in the following chapters.

Hypotheses 1), that PPSM has advantages in data rate, working range and energy efficiency compared with conventional *Passive Impedance Modulation* and 2), that the power loss is mainly due to resistance in the primary circuit, were tested in Chapter 3. They are generally proved to be true except for the claim on the working range of PPSM, which is comparable to that in *Impedance Modulation* rather than outperforming it.

Hypothesis 3), that the transient waveform generated by PPSM is suitable for demodulation within the required working range, was proved to be true in theory in Chapter 5 and in the real system in Chapter 9.

Hypothesis 4), that the switch closing action only changes the i_2 phase and will not affect any other currents and voltages, was tested in Appendix 5. At weak coupling,

the hypothesis stands. When the coupling is greater, $v_{C1}(t_0)$ has a greater value. However, to estimate the initial conditions for stage 3 (see Chapter 4), this hypothesis can still be used.

Hypothesis 5), that the circuit parameters optimised for power transfer efficiency are also good for signalling, was proved to be true in Chapter 5 and in the design chapters.

10.3 The author's contributions

1. A literature review of data transmission methods in biotelemetry was presented. Passive transmission, which had not been thoroughly reviewed previously, was summarised in Chapter 1.

2. A detailed literature review of the inductively coupled RF power link for implant neuroprostheses was presented. In designing an optimised RF power link, the author contributes several improvements (see Section 2.2, Chapter 2).

3. The mechanism of *Passive Phase Shift Modulation* was introduced. Comparison between *Impedance Modulation* and PPSM on synchronisation, working distance, energy consumption and speed were conducted using PSpice simulation. These issues have never been addressed before.

4. *Passive Phase Shift Modulation* was theoretically analysed in great depth. The analytical function of transient response for the circuit configuration concerned was solved. It has not been found in the literature in the related fields before.

5. A novel procedure, which separates the modulation into three stages, helps greatly in simplifing the analysis, so does the treatment, which groups the initial conditions according to their destinations to turn the multi-input problem into a single input problem.

6. The little known Pierce's method of deriving analytical solutions for the inductive coupled circuits was dug out [81]. However, Pierce solved the

problem for the series-tuned primary, series-tuned secondary circuit configuration. The author used his method to derive the analytical solution for our circuit configurations (the primary is series tuned and secondary parallel tuned). Although the procedure and the result were not adopted in the main body of the thesis due to complexity, the solution is a contribution to existing knowledge.

7. A method combining Laplace transformation and numerical partial-fraction expansion to analyse the transient response of inductively coupled circuits with a higher number of modes was developed. It arrives at the same results as the analytical solution (Pierce's method) does, but is more straightforward. Furthermore, this method is more generic. It can be applied to the similar problems in other fields, while Pierce's method is for inductive coupled circuits only because it relies on physical relations of the parameters to simplify the equations.

8. A PPSM prototype was designed, constructed and tested. The transmitter was modified from Tim Perkins' design for the LARSI system. The implant and external circuits are original.

9. In both theory and practice, *Passive Phase Shift Modulation* was proved a satisfactory method for high-speed data transmission in implantable closed-loop neuroprostheses.

10. The application for *Passive Phase Shift Modulation* may extend to the RFID field (see below).

10.4 Future work, limitation and further applications

10.4.1 Future work

The theoretical study of PPSM, in the author's opinion, is completed in this thesis. The electronic prototype designed in this thesis can be easily adapted by a closed-loop implantable neuroprosthesis with only a few modifications. For example,

coordinating the digital logic with the other parts of the neuroprosthesis to avoid stimulation and recording being carried out simultaneously.

The major amendment is to design a coupling compensation circuit to maintain the implant voltage when the coil distance changes. The design principle was discussed in Chapter 6. For electronic realisation, see [77].

When the author designed the bit synchronisation in Section 8.3, Chapter 8, Digital Phase-Locked Loop CD74HC297 was used. Its modulo K is set by external programmable pins, can only be 2^3, 2^4, etc. However, in this system K = 18 is preferred in order to minimise jitter. Therefore, in future a new DPLL chip with K being flexibly programmed shall be considered. Furthermore, DPLL and word synchronisation logic can be implemented into a single logic device to make the system more compact.

Besides, as mentioned in Chapter 9, further measurements to evaluate the performance of bit and word synchronisation are necessary. Error rate, PLL lock range, error recovery time, capture time, etc, shall be investigated experimentally to estimate the reliability of the system.

10.4.2 Limitation

Passive Phase Shift Modulation is mostly suitable for a medium range inductive coupling system ($0.01 \leq k < 0.16$). In close range (higher k), the waveform beats. Demodulation might become difficult. At a greater range, the modulation is too small to be detectable unless the detecting circuit is highly sensitive.

10.4.3 Further applications

The method developed in this thesis for analysing the transient response of inductively coupled circuits with a higher number of modes may be useful for similar problems in other fields.

Apart from neuroprosthesis and biotelemetry areas, *Passive Phase Shift Modulation* might be very useful in *Radio Frequency Identification* tags (RFID). The working principle of RFID is similar to biotelemetry, except that the remote unit (equivalent to implant circuit) does not contain a sensor, but rather has the data pre-

stored. Currently, RFID is gaining popularity in the commercial applications of contactless smart cards, fare systems for public transport, access control, container identification, goods transport and industrial automation. Improving the data transmission rate in RFID will contribute greatly to productivity.

10.5 Summary

In conclusion, this thesis presents the development of a novel passive modulation method PPSM. It achieves a higher bit rate/carrier frequency ratio than previous methods, and improves the information capacity the RF signal can carry. It enables transmission of signals with large bandwidth without necessarily increasing the frequency of a carrier. It is a satisfactory method for designing a practical feed-back controlled neuroprosthesis.

Appendixes

Appendix 1 Frequency choices

Besides the restrictions imposed by government regulations, cost and availability of the technology, a number of factors influence the choice of frequency[1].

Factors suggesting a high frequency

1. Antenna efficiency: in far field operation, an antenna is more effective if its size is comparable to the wavelength. So working on higher frequency (equal to shorter wavelength), the antenna, therefore, together with the remote unit, can be made compact.

2. Detection sensitivity: given same data bandwidth, high carrier frequency enables use of narrow band filter with higher Q (quality factor)[2], so that the weaker signal can be picked up, thus increasing the detection sensitivity, or the range.

3. Higher frequency allows wider data bandwidth thus fast data transmission speed.

4. Suitable technology, commercial components, and receivers might be readily available at some frequency band used by the telecommunication field.

Factors suggesting a low frequency

5. Attenuation by tissues increases with the frequency. Therefore, for implantable devices, lower frequency is preferred.

6. High frequency waveform is more likely reflected, or scattered by the surrounding objects. The environment where telemetry is working must be taken into account.

[1] Based on Mackay's book [68] and on the author's discussion with the supervisor Tim Perkins.
[2] Q = operating frequency/bandwidth [97].

7. The resonant circuit in low frequency unit has large tuning capacitor, is less affected by small stray capacitances (such as hand capacitance), thus tends to be more stable.

8. Working on a low clock frequency reduces power consumption.

The choice of frequency is a compromise between those factors. From the signal transmission point of view only, high frequency is used more often in the external worn devices working on medium and long-range. For implantable devices, the tissue absorption rate must be taken into account, but need not be very critical. Many researchers choose an operating frequency because there are commercially available receivers (27+ MHz). However, if power is also to be transmitted via RF, the frequency choice will be more restricted (i.e. lower, about 0.2 to 5 MHz) in order to achieve high power efficiency.

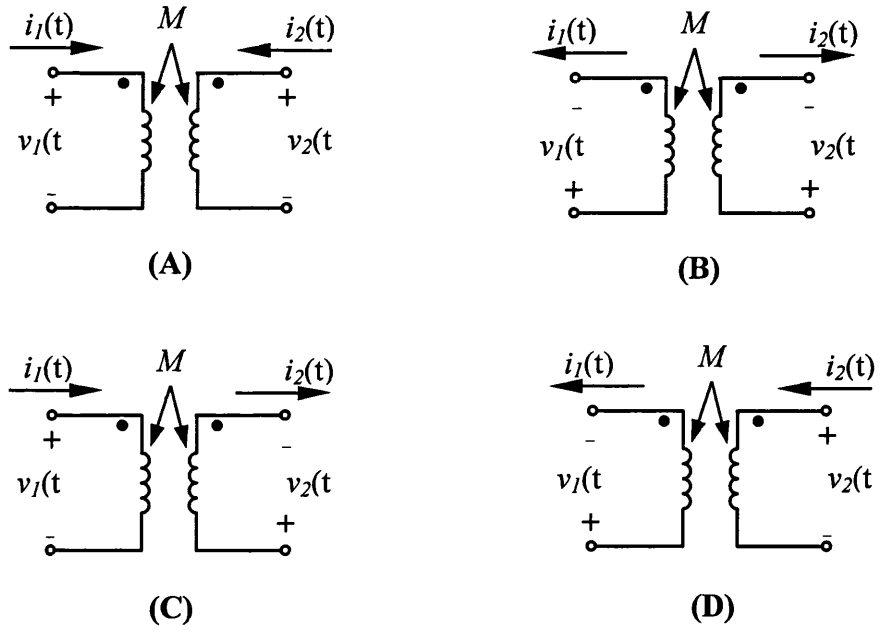
Summary

The frequency chosen for this work, i.e. 4 MHz, is at the upper end of the frequency range for good power transfer efficiency. This allows a high data rate without unduly compromising the power transfer efficiency.

Appendix 2 The rules for correct assignment of the sign of mutual inductance term for a pair of coupled coils[1]

The rule stated in terms of currents: when the current reference directions both point toward or point away from a dotted terminal, the mutual coupling is additive; otherwise, the coupling is subtractive.

Or the rule stated in terms of voltages: when the voltage reference marks are both positive or both negative at the dotted terminals, mutual inductance is additive; otherwise, it is subtractive.



According to the rule, the element equations for a pair of coupled coils in figure A and B are

$$Coil\ 1:\ v_1(t) = L_1 \frac{di_1(t)}{dt} + M \frac{di_2(t)}{dt}$$

$$Coil\ 2:\ v_2(t) = M \frac{di_1(t)}{dt} + L_2 \frac{di_2(t)}{dt}$$

[1] From book by [98] (p335)

For the coils in figure C and D, the equations are

$$Coil\ 1:\ v_1(t) = L_1 \frac{di_1(t)}{dt} - M \frac{di_2(t)}{dt}$$

$$Coil\ 2:\ v_2(t) = -M \frac{di_1(t)}{dt} + L_2 \frac{di_2(t)}{dt}$$

Appendix 3 Measurement of coupling coefficient k[1]

The circuit diagram for measurement is as below:

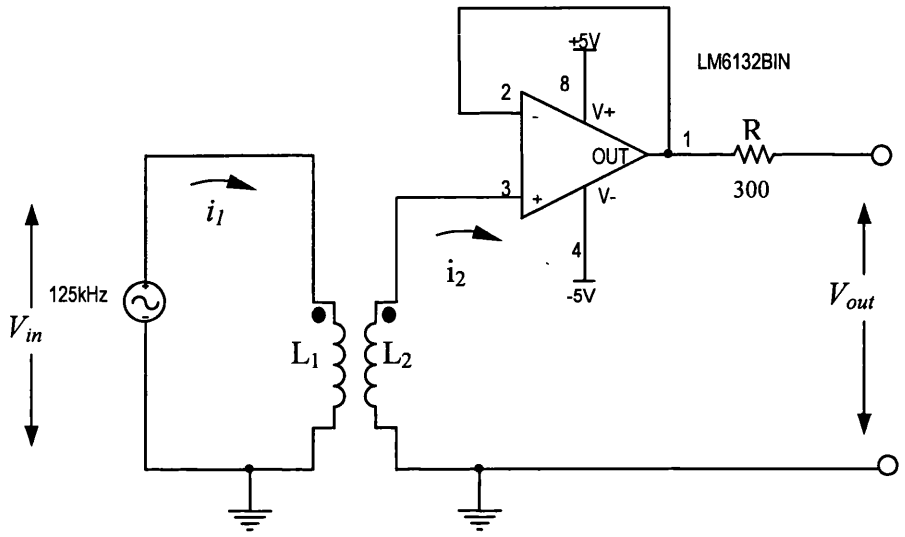


Fig.A 3.1 Circuit diagram for measuring coupling coefficient.

There are relations:

$$\left.\begin{aligned} L_1\frac{di_1}{dt} - M\frac{di_2}{dt} &= V_{in} \\ -M\frac{di_1}{dt} + L_2\frac{di_2}{dt} + R_1 i_2 &= V_{out} \end{aligned}\right\}$$

In which V_{in}, V_{out} are the amplitude of the input and the output respectively.

Because $i_2 = 0$, $\frac{di_2}{dt} = 0$, so that,

$$k = A_k \frac{V_{out}}{V_{in}}\sqrt{\frac{L_1}{L_2}}$$

Where A_k is the correction factor, there is

[1] Modified from [33] Page 99, used by Temic Semiconductor GmbH, Heilbronn.

$$A_k = 2 - \frac{1}{1-(\omega^2 C_{TOT} L_2)}, C_{TOT} = C_{PARA} + C_{CABLE} + C_{PROBE}$$

C_{PARA} is the parasit capacitance on the circuit board, C_{CABLE} and C_{PROBE} are the capacitance of the measuring cable and probe respectively.

Appendix 4 Physical meanings of Ω, Ω_1, Ω_2, Ω', Ω'', ω_1, ω_2, ω_T, ω', ω'', f_0, f_1, f_2, f_{d1}, f_{d2}, f_d', f_d'', α_1, α_2, α_T, α', α'' and $1/\alpha_1$, $1/\alpha_2$, $1/\alpha'$, $1/\alpha''$

A.4.1 Introduction

In Chapters 4 and 5, Appendixes 5 and 7, several symbols appear with different subscripts, namely Ω, Ω_1, Ω_2, Ω', Ω'', ω_1, ω_2, ω_T, ω', ω'', f_0, f_1, f_2, f_{d1}, f_{d2}, f_d', f_d'', α_1, α_2, α_T, α', α'' and $1/\alpha_1$, $1/\alpha_2$, $1/\alpha'$, $1/\alpha''$. This appendix is to clarify their physical meanings.

Before proceeding, please note that the LC circuits being discussed in this appendix are all highly oscillatory, which means the over-damped cases will not be considered.

A.4.2 Ω and f_0

Ω is the angular frequency of the driving force, $v_s(t) = E \cos(\Omega t)$. Its corresponding frequency is $f_0 = \Omega / 2\pi$.

A.4.3 Ω_1, ω_1, f_1, f_{d1}, α_1, $1/\alpha_1$

Considering the primary circuit alone and uninfluenced by the secondary, it is a series tuned RLC circuit (Fig.A 4. 1).

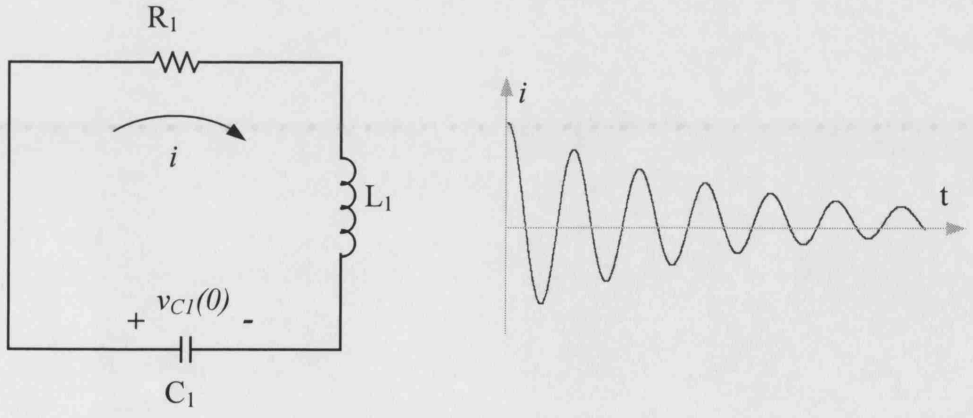


Fig.A 4. 1 The primary circuit on its own.

If C_1 (or L_1) is charged initially and left to discharge freely, the circuit becomes oscillatory. If $R_1 = 0$, it oscillates at an **undamped angular frequency Ω_1**, which is

$$\Omega_1 = \frac{1}{\sqrt{L_1 C_1}}$$

Practically, however, $R_1 \neq 0$. The oscillation decays to zero. The **damping constant α_1** indicates the rate of decay. Also the oscillating frequency is smaller, represented by **damped angular frequency ω_1**. Thus

$$\alpha_1 = \frac{R_1}{2L_1} \text{ or } \alpha_1 = \frac{\Omega}{2Q_1}$$

and

$$\omega_1^2 = \Omega_1^2 - \alpha_1^2$$

f_1 is the undamped frequency corresponding to Ω_1,

$$f_1 = \Omega_1 / 2\pi$$

f_{d1} is the damped frequency corresponding to ω_1,

$$f_{d1} = \omega_1 / 2\pi$$

α_1's reciprocal **$1/\alpha_1$** is the **decay time constant.**

A.4.4 Ω_2, ω_2, f_2, f_{d2}, α_2, $1/\alpha_2$

Similarly, considering the secondary circuit alone and uninfluenced by the primary. The **undamped angular frequency** is **Ω_2**, given by

$$\Omega_2 = \frac{1}{\sqrt{L_2 C_2}}$$

Because the secondary is parallel tuned, the **damping constant** is

$$\alpha_2 = \frac{1}{2R_2C_2} \text{ or } \alpha_2 = \frac{\Omega}{2Q_2}$$

The **damped angular frequency** is

$$\omega_2^2 = \Omega_2^2 - \alpha_2^2$$

***f_2* is the undamped frequency** corresponding to Ω_2,

$$f_2 = \Omega_2 / 2\pi$$

***f_{d2}* is the damped frequency** corresponding to ω_2,

$$f_{d2} = \omega_2 / 2\pi$$

$1/\alpha_2$ is **the decay time constant** for the secondary circuit.

A.4.5 Describing $1/\alpha_1$, $1/\alpha_2$, ω_1, ω_2 by Ω, Q_1, Q_2

In this thesis, Ω_1 and Ω_2 are let to be equal to the frequency of the driving force Ω, so there are

$$\Omega = \Omega_1 = \Omega_2 \quad \text{or} \quad \Omega = \frac{1}{\sqrt{L_1 C_1}} = \frac{1}{\sqrt{L_2 C_2}}$$

Normally RLC circuit is described by the quality factor Q. The quality factor for the primary circuit is Q_1, which is $Q_1 = \frac{\Omega L_1}{R_1}$; the quality factor for the secondary circuit is Q_2, which is $Q_1 = \Omega R_2 C_2$. Therefore, $1/\alpha_1$, $1/\alpha_2$, ω_1, ω_2 can be described as

$$1/\alpha_1 = 2Q_1/\Omega, \text{ and } \omega_1 = \frac{1}{2\pi}\sqrt{\Omega^2 - (\frac{\Omega}{2Q_1})^2}$$

$$1/\alpha_2 = 2Q_2/\Omega, \text{ and } \omega_2 = \frac{1}{2\pi}\sqrt{\Omega^2 - (\frac{\Omega}{2Q_2})^2}$$

A.4.6 α_T and ω_T

ω_T and α_T are introduced in Appendix 5 during the analysis of stage 2. They are the damping constant and the damped angular frequency when the primary circuit couples to a terminal-shorted inductor. The expressions will be found in Appendix 5.

A.4.7 Ω', Ω'', ω', ω'', f_d', f_d'', α', α'' and $1/\alpha'$, $1/\alpha''$

When a tuned primary circuit approaches a tuned secondary circuit, the two circuits begin to influence each other. If one or more of L_1, C_1, L_2, and C_2 is charged initially and left to discharge freely, two oscillations will occur in both primary and secondary circuits. They are inseparatable, and always appear together. Therefore the currents and voltages in both circuits are doubly periodic, oscillating at damped angular frequencies ω' and ω''. Each oscillation has its own damping constants, a' for ω' and a'' for ω'', there are

$$\omega'^2 = \Omega'^2 - a'^2$$

$$\omega''^2 = \Omega''^2 - a''^2$$

Ω' and Ω'' are the corresponding **undamped angular frequencies. f_d' and f_d''** are corresponding frequencies to ω' and ω''. Thus

$$f_d' = \omega' /2\pi \quad \text{and} \quad f_d'' = \omega'' /2\pi$$

and $1/\alpha'$ and $1/\alpha''$ are corresponding time constants to α' and α''.

A.4.8 Summary

Table A. 4.1 below summarises the symbols and the corresponding circuits they describe. Table A. 4.2 summarises the definition of those symbols.

Table A. 4.1 Symbols and corresponding circuits described

Symbols	**Circuits or source described**
Ω and f_0	Driving e.m.f. force
Ω_1, ω_1, f_1, f_{d1}, α_1, $1/\alpha_1$	The primary circuit alone.
Ω_2, ω_2, f_2, f_{d2}, α_2, $1/\alpha_2$	The secondary circuit alone
α_T and ω_T	The primary couples to a terminal-shorted inductor, the situation in stage 2.
Ω', Ω'', ω', ω'', f_d', f_d'', α', α'' and $1/\alpha'$, $1/\alpha''$	The tuned primary circuit inductively couples to a tuned secondary, the situation in stage 3.

Table A. 4.2 Definition of the symbols

Symbols	**Definition**
Ω, Ω_1, Ω_2, Ω', Ω'',	Undamped angular frequencies
ω_1, ω_2, ω_T, ω', ω''	Damped angular frequencies
f_0	Frequency of driving force corresponding to Ω
f_1, f_2	Undamped frequencies corresponding to Ω_1, Ω_2
f_{d1}, f_{d2}	Damped frequencies corresponding to ω_1, ω_2
f_d', f_d''	Damped frequencies corresponding to ω', ω''
α_1, α_2, α_T, α', α''	Damping constants
$1/\alpha_1$, $1/\alpha_2$, $1/\alpha_T$, $1/\alpha'$, $1/\alpha''$	Time constants

Appendix 5 Circuit response in stage 2

A.5.1 Introduction

This appendix is the amendment of Section 4.4.2, Chapter 4. It aims to understand the effect of the switching action, to test the hypothesis about stage 2, to evaluate the $i_1(t)$, $v_{C1}(t)$ and $i_2(t)$ values at $t = t_0$ which are the initial conditions for stage 3.

The hypothesis states that because the duration of the period between $t_{-1} \sim t_0$ (stage 2) is short, the only significant effect of shorting the terminals of the secondary coil is that it results in an inverted phase of $i_2(t)$ at $t = t_0$, and the signals in the primary circuit are not affected, after the switch opens they will carry on as if nothing had happened. If this hypothesis is tested to be true, the values of $i_1(t_0)$, $v_{C1}(t_0)$ and $i_2(t_0)$ can be estimated from the steady-state response, which is much more simple.

In this appendix, firstly the mathematic expression of $i_1(t)$, $v_{C1}(t)$ and $i_2(t)$ for stage 2 will be found by Laplace-transformation which solves the differential equations that describe the response of the circuit of stage 2; they are then compared with the response of the steady-state to test the hypothesis, and finally $i_1(t_0)$, $v_{C1}(t_0)$, $i_2(t_0)$ and $v_{C2}(t_0)$ will be evaluated.

The signal status at $t = t_{-1}$ derived in the section 4.3, Chapter 4 are the initial conditions for stage 2. For convenient reference, they are rewritten here

$$\left.\begin{aligned} & i_1(t_{-1}) = 0 \\ & v_{C1}(t_{-1}) = -V_{C1max} \\ & i_2(t_{-1}) = I_{2max} \sin(\angle I_2 - \angle I_1) \\ & v_{C2}(t_{-1}) = 0 \\ & v_s(t_{-1}) = E\cos(\frac{3\pi}{2} - \angle I_1) \end{aligned}\right\} \quad \text{------Eq.A 5.1}$$

Following relations in the steady-state are rewritten here also

$$V_{C1\max} = \frac{1}{\Omega C_1} I_{1\max} \qquad \text{------Eq.A 5.2}$$

$$\frac{I_{2\max}}{I_{1\max}} = k\sqrt{\frac{C_2}{C_1}(1+Q_2^2)} \qquad \text{------Eq.A 5.3}$$

$$I_{1\max} = |I_1| = \frac{C_1 Q_1 \Omega}{\sqrt{(1+k^2 Q_1 Q_2)^2 + k^4 Q_1^2}} E \qquad \text{------Eq.A 5.4}$$

$$\angle I_1 = Arc\tan\left(\frac{1}{\frac{1}{k^2 Q_1} + Q_2}\right) \qquad \text{------Eq.A 5.5}$$

$$\angle I_2 - \angle I_1 = Arc\tan(Q_2) \qquad \text{------Eq.A 5.6}$$

Furthermore, from Eq.A 5.6 $i_2(t_{-1})$ in Eq.A 5.1 can be represented as

$$i_2(t_{-1}) = \frac{Q_2}{\sqrt{1+Q_2^2}} I_{2\max} \qquad \text{------Eq.A 5.7}$$

Regarding all the initial conditions in Eq.A 5.1 as the inputs, stage 2 can be considered independently from the previous stage. For convenience, arbitrarily let $t_{-1}= 0$, all above equations are still valid. The external force $v_s(t)$ will not be affected by the changes of the circuit configuration, but its expression in stage 1 needs to be adjusted for the new time origin. Because it starts with a phase angle $(\frac{3\pi}{2} - \angle I_1)$ at t_{-1}, the adjusted expression is

$$v_s(t) = E\cos(\Omega t - \frac{\pi}{2} - \angle I_1), \quad t \geq t_{-1} \qquad \text{------Eq.A 5.8}$$

The expression of $i_1(t)$, $v_{C1}(t)$ and $i_2(t)$ in the steady-state will be used for the comparison, so they are also adjusted for the new time origin. From the Section 4.3, Chapter 4, we know they have the phase angles $\frac{3\pi}{2}$, π and $(\frac{3\pi}{2}+\angle I_2-\angle I_1)$ respectively at $t = t_{-1}$, so the adjusted formulae are

$$i_1(t) = I_{1\max}\cos(\Omega t+\frac{3\pi}{2}) \qquad \text{------Eq.A 5.9}$$

$$v_{C1}(t) = V_{C1\max}\cos(\Omega t+\pi) \qquad \text{------ Eq.A 5.10}$$

$$i_2(t) = I_{2\max}\cos(\Omega t+\frac{3\pi}{2}+\angle I_2-\angle I_1) \qquad \text{------ Eq.A 5.11}$$

A.5.2 Differential equation

Following the Section 4.4.2, Chapter 4, rewriting the differential equation for stage 2:

$$\left.\begin{aligned} R_1 i_1 + L_1\frac{di_1}{dt}+\frac{1}{C_1}\int i_1 dt - M\frac{di_2}{dt} = v_s(t) \\ -M\frac{di_1}{dt}+L_2\frac{di_2}{dt}=0 \end{aligned}\right\} \qquad \text{------ Eq.A 5.12}$$

A.5.3 Laplace transformation

Let the Laplace transformation of $i_1(t)$, $i_2(t)$ and $v_s(t)$ be $I_1(s)$, $I_2(s)$ and $V_s(s)$ respectively, the Laplace transform of Eq.A 5.12 is

$$\left.\begin{aligned} R_1 I_1(s)+L_1 s I_1(s)+\frac{1}{C_1 s}I_1(s)+\frac{v_{C1}(t_{-1})}{s}-[M s I_2(s)-M i_2(t_{-1})]=V_s(s) \\ -M s I_1(s)+L_2 s I_2(s)-L_2 i_2(t_{-1})=0 \end{aligned}\right\}$$

-------Eq.A 5.13

In which $v_{C1}(t_{-1})$, $i_2(t_{-1})$ and the impressed force $v_s(t)$ ($t \geq t_{-1}$) are non-zero initial conditions. For the rules of the Laplace transform with initial conditions, see Appendix 6. Rearranging Eq.A 5.13 gives

$$\left.\begin{aligned}\left(R_1 + L_1 s + \frac{1}{C_1 s}\right) I_1(s) - M s I_2(s) &= V_s(s) - \frac{v_{C1}(t_{-1})}{s} - M i_2(t_{-1}) \\ -M s I_1(s) + L_2 s I_2(s) &= L_2 i_2(t_{-1})\end{aligned}\right\}$$

-------Eq.A 5.14

The determinant of Eq.A 5.14 is

$$\Delta(s) = \begin{vmatrix} R_1 + L_1 s + \dfrac{1}{C_1 s} & -Ms \\ -Ms & L_2 s \end{vmatrix}$$

Find $I_1(s)$, $I_2(s)$ by Cramer's rule

$$I_1(s) = \frac{\Delta_1(s)}{\Delta(s)} = \frac{\begin{vmatrix} V_s(s) - \dfrac{v_{C1}(t_{-1})}{s} - M i_2(t_{-1}) & -Ms \\ L_2 i_2(t_{-1}) & L_2 s \end{vmatrix}}{\Delta(s)}$$

$$I_2(s) = \frac{\Delta_2(s)}{\Delta(s)} = \frac{\begin{vmatrix} R_1 + L_1 s + \dfrac{1}{C_1 s} & V_s(s) - \dfrac{v_{C1}(t_{-1})}{s} - M i_2(t_{-1}) \\ -Ms & L_2 i_2(t_{-1}) \end{vmatrix}}{\Delta(s)}$$

After matrix manipulation, they become

$$I_1(s)=\frac{\dfrac{-C_1\,\Omega^2}{1-k^2}\,v_{C1}(t_{-1})}{s^2+\dfrac{\Omega}{(1-k^2)\,Q_1}\,s+\dfrac{\Omega^2}{1-k^2}}+\frac{\dfrac{C_1\,\Omega^2\,s}{1-k^2}\,V_s(s)}{s^2+\dfrac{\Omega}{(1-k^2)\,Q_1}\,s+\dfrac{\Omega^2}{1-k^2}}$$

-------Eq.A 5.15

$$I_2(s)=\frac{\dfrac{-k}{(1-k^2)\sqrt{L_1 L_2}}\,v_{C1}(t_{-1})}{s^2+\dfrac{\Omega\,s}{(1-k^2)\,Q_1}+\dfrac{\Omega^2}{1-k^2}}+\frac{\dfrac{k\,s}{(1-k^2)\sqrt{L_1 L_2}}\,V_s(s)}{s^2+\dfrac{\Omega\,s}{(1-k^2)\,Q_1}+\dfrac{\Omega^2}{1-k^2}}+\frac{i_2(t_{-1})}{s}$$

-------Eq.A 5.16

In which $\Omega^2=\dfrac{1}{L_1C_1}$, $Q_1=\dfrac{\Omega L_1}{R_1}$, $k=\dfrac{M}{\sqrt{L_1 L_2}}$

Eq.A 5.15 is the Laplace transform of i_1(t) for t > t_{-1}. The first term results from the input $v_{C1}(t_{-1})$ and the second term from input by the external driving voltage source. The superposition theorem states that the total circuit response is the sum of the individual responses caused by each input acting alone. According to the theorem, there should be a third term contributed from $i_2(t_{-1})$ in Eq.A 5.15. However, $i_2(t_{-1})$ is cancelled during the equation manipulation. This can be explained by the fact that once the secondary coil's terminals are shorted, $i_2(t_{-1})$ has nowhere to discharge, therefore it is kept constant and $\dfrac{di_2(t_{-1})}{dt}=0$. As unchanging current cannot generate e.m.f.s, it does not contribute to the AC current in both the primary and secondary circuits. (Note that although the initial current $i_2(t_{-1})$ does not make a contribution, the secondary circuit still influences the primary circuit via k and L_2).

Now consider i_1, v_{C1} and i_2 individually.

A.5.4 Response of i_1(t)

Let i_{1by_vc1} be the response resulting from $v_{C1}(t_{-1})$ and i_{1by_vs} be the response resulting from v_s(t) in stage 2. From Eq.A 5.15, we know i_1(t) should be the sum of i_{1by_vc1} and i_{1by_vs}, so

$$i_1(t) = i_{1by\_vc1} + i_{1by\_vs}$$

In the following sections, i_{1by_vc1} and i_{1by_vs} will be derived separately, then sum them to form the complete response of i_1(t), and finally normalise i_1(t) in respect to I_{1max}.

A.5.4.1 i_{1by_vc1} caused by $v_{C1}(t_{-1})$

In Eq.A 5.15, the response caused by $v_{C1}(t_{-1})$ is

$$I_1(s)_{by\_v_{C1}} = \frac{\dfrac{-C_1\,\Omega^2}{1-k^2}\,v_{C1}(t_{-1})}{s^2 + \dfrac{\Omega}{(1-k^2)\,Q_1}\,s + \dfrac{\Omega^2}{1-k^2}}$$

Factorising the denominator, results in

$$I_1(s)_{by\_v_{C1}} = \frac{\dfrac{-C_1\,\Omega^2}{1-k^2}\,v_{C1}(t_{-1})}{(s+a_T - j\omega_T)\,(s+a_T + j\omega_T)}$$

$$= \frac{C_1\,\Omega\,Q_1\,v_{C1}(t_{-1})}{\sqrt{-1+4\,(1-k^2)\,Q_1^2}}\left(\frac{j}{(s+a_T - j\omega_T)} + \frac{-j}{(s+a_T + j\omega_T)}\right)$$

------ Eq.A 5.17

Where

$$\alpha_T = \frac{\Omega}{2\,Q_1\,(1-k^2)}$$

------ Eq.A 5.18

$$\omega_T = \Omega \frac{\sqrt{4\,(1-k^2)\,Q_1^2 - 1}}{2\,Q_1\,(1-k^2)} \qquad \text{------ Eq.A 5.19}$$

α_T and ω_T are the damping constant and the damped angular frequency for the circuit configuration studied in stage 2.

Performing inverse transformation on Eq.A 5.17 yields

$$i_1(t)_{by\_v_{C1}} = \frac{2\,C_1\,\Omega\,Q_1\,v_{C1}(t_{-1})}{\sqrt{-1+4\,(1-k^2)\,Q_1^2}}\; e^{-\alpha_T t}\; \cos\left(\omega_T\, t + \frac{\pi}{2}\right) \qquad \text{------ Eq.A 5.20}$$

A.5.4.2 i_{1by_vs} caused by $v_s(t)$ ($t \geq t_{-1}$)

In Eq.A 5.15, the response caused by v_s(t) alone is

$$I_1(s)_{by\_vs} = \frac{\frac{C_1\,\Omega^2\,s}{1-k^2}\,V_s(s)}{s^2 + \frac{\Omega}{(1-k^2)\,Q_1}\,s + \frac{\Omega^2}{1-k^2}} \qquad \text{------ Eq.A 5.21}$$

From Eq.A 5.8 we know the external source is

$$v_s(t) = E\cos(\Omega t - \frac{\pi}{2} - \angle I_1)$$

$$= E\sin(\Omega t - \angle I_1)$$

$$= E\sin(\Omega(t - \frac{\angle I_1}{\Omega}))$$

$$= E\sin(\Omega\, t') \qquad \text{------ Eq.A 5.22}$$

In which

$$t' = t - \frac{\angle I_1}{\Omega} \qquad \text{------ Eq.A 5.23}$$

In order to simplify the manipulation, we will solve the response in respect to t' and later shift the time back to t by Eq.A 5.23. Hence, the Laplace transform of Eq.A 5.22 in the t'-domain is $V_s(s) = \frac{\Omega E}{s^2+\Omega^2}$. Substituting it into Eq.A 5.21 and factoring the denominator yields

$$I_1(s)_{by\_vs} = \frac{\frac{C_1 \Omega^3 E s}{1-k^2}}{(s-j\Omega)(s+j\Omega)(s+a_T-j\omega_T)(s+a_T+j\omega_T)} \quad \text{------ Eq.A 5.24}$$

Where α_T and ω_T are as Eq.A 5.18 and Eq.A 5.19. The partial fraction expansion of Eq.A 5.24 is

$$I_1(s)_{by\_vs} = \frac{g_1}{(s-j\Omega)} + \frac{g_1^*}{(s+j\Omega)} + \frac{g_2}{(s+a_T-j\omega_T)} + \frac{g_2^*}{(s+a_T+j\omega_T} \quad \text{------ Eq.A 5.25}$$

The residues g_1, g_1*, g_2, and g_2* are found using the cover-up algorithm [98]:

$$g_1 = (s-j\Omega)\, I_1(s)\Big|_{s=j\Omega} = \frac{C_1 Q_1 \Omega E}{2(1+k^4 Q_1^2)}(k^2 Q_1 - j)$$

$$g_1^* = (s+j\Omega)\, I_1(s)\Big|_{s=-j\Omega} = \frac{C_1 Q_1 \Omega E}{2(1+k^4 Q_1^2)}(k^2 Q_1 + j)$$

$$g_2 = (s+\alpha_T - j\omega_T)\, I_1(s)\Big|_{s=-\alpha_T+j\omega_T}$$

$$= \frac{C_1 Q_1^2 \Omega E}{2(1+k^4 Q_1^2)}\left(-k^2 + j\frac{2-k^2}{\sqrt{-1+4(1-k^2)Q_1^2}}\right)$$

$$g_2^* = (s+\alpha_T + j\omega_T)\, I_1(s)\Big|_{s=-\alpha_T-j\omega_T}$$

$$= \frac{C_1 Q_1^2 \Omega E}{2(1+k^4 Q_1^2)} \left(-k^2 - j \frac{2-k^2}{\sqrt{-1+4(1-k^2) Q_1^2}} \right)$$

The inverse transform of Eq.A 5.25 to the t'-domain gives

$$i_{1by\_vs}(t') = 2|g_1|\cos(\Omega t' + \angle g_1) + 2|g_2| e^{-\alpha_T t'} \cos(\omega_T t' + \angle g_2) \quad \text{------ Eq.A 5.26}$$

In which

$$|g_1| = \frac{C_1 Q_1 \Omega E}{2\sqrt{k^4 Q_1^2 + 1}} \quad \text{------ Eq.A 5.27}$$

$$\angle g_1 = Arc\tan\left(\frac{-1}{k^2 Q_1} \right) \quad \text{------ Eq.A 5.28}$$

$$= 2\pi - Arc\tan\left(\frac{1}{k^2 Q_1} \right)$$

$$|g_2| = C_1 Q_1^2 \Omega E \sqrt{\frac{1-k^2}{(k^4 Q_1^2 + 1)(-1+4(1-k^2) Q_1^2)}} \quad \text{------ Eq.A 5.29}$$

$$\angle g_2 = Arc\tan\left(\frac{\dfrac{(2-k^2)\sqrt{-1+4(1-k^2) Q_1^2}}{-1+4(1-k^2) Q_1^2}}{-k^2} \right)$$

$$= \pi + Arc\tan\left(\frac{-(2-k^2)}{k^2 \sqrt{-1+4(1-k^2) Q_1^2}} \right) \quad \text{------ Eq.A 5.30}$$

(Beware $\angle g_2$ is in the second quadrant, so we should add π)

Shifting from the t'-domain to the t-domain by Eq.A 5.23 obtains

$$i_{1by\_vs}(t-\frac{\angle I_1}{\Omega}) =$$

$$2\,|g_1|\cos(\Omega\ (t-\frac{\angle I_1}{\Omega})+\angle g_1)+2\,|g_2|\,e^{-\alpha_T(t-\angle I_1/\Omega)}\cos(\omega_T\ (t-\frac{\angle I_1}{\Omega})+\angle g_2)$$

Rearranging gives

$i_{1by\_vs}(t) =$

$$\underbrace{2\,|g_1|\cos(\Omega t-\angle I_1+\angle g_1)}_{\text{steady-state}}+\underbrace{2\,|g_2|e^{\alpha_T\angle I_1/\Omega}\,e^{-\alpha t}\cos\left(\omega_T\ t-\frac{\omega_T\ \angle I_1}{\Omega}+\angle g_2\right)}_{\text{natural response}}$$

------ Eq.A 5.31

Eq.A 5.31 is the response caused by the driving source $v_s(t) = E\cos(\Omega t-\frac{\pi}{2}-\angle I_1)$ alone. The first term is the steady-state, to which $i_1(t)$ would finally settle after the transient period. The second term is a damped cosine due to the natural response excited by the external driving force. It would die away after a short period.

A.5.4.3 Total response of $i_1(t)$ in time domain

Combining Eq.A 5.20 and Eq.A 5.31, the total inverse transform of Eq.A 5.15 is

$$i_1(t) = \frac{2\,C_1\,\Omega\,Q_1\,v_{C1}(t_{-1})}{\sqrt{-1+4(1-k^2)Q_1^2}}e^{-\alpha_T t}\cos\left(\omega_T\,t+\frac{\pi}{2}\right)+$$

$$2\,|g_1|\cos(\Omega t-\angle I_1+\angle g_1)+2|g_2|e^{\alpha_T\angle I_1/\Omega}\,e^{-\alpha_T t}\cos(\omega_T\,t-\frac{\omega_T\,\angle I_1}{\Omega}+\angle g_2)$$

------ Eq.A 5.32

Where α_T, ω_T, $|g_1|$, $|g_2|$, $\angle g_1$ and $\angle g_2$ are represented by Eq.A 5.18, Eq.A 5.19, Eq.A 5.27, Eq.A 5.29, Eq.A 5.28, Eq.A 5.30 respectively. $\angle I_1$ is from Eq.A 5.5. $v_{C1}(t_{-1})$ from Eq.A 5.1.

A.5.4.4 Normalise $i_1(t)$ to I_{1max}

The amplitude of the first term in Eq.A 5.32 contains $v_{C1}(t_{-1})$, where $v_{C1}(t_{-1}) = -V_{C1max}$. From Eq.A 5.2, we know $V_{C1max} = \frac{1}{\Omega C_1} I_{1\max}$, therefore

$$v_{C1}(t_{-1}) = -V_{C1\max} = -\frac{1}{\Omega C_1} I_{1\max} \qquad \text{------ Eq.A 5.33}$$

The amplitudes of the 2nd and 3rd terms in Eq.A 5.32 include the magnitude of the external source E. Rearranging Eq.A 5.4, we have

$$E = \frac{\sqrt{(1+k^2 Q_1 Q_2)^2 + k^4 Q_1^2}}{C_1 Q_1 \Omega} I_{1\max} \qquad \text{------ Eq.A 5.34}$$

Substituting Eq.A 5.33 and Eq.A 5.34 into Eq.A 5.32, the $i_1(t)$ response can be represented by I_{1max}, k, Q_1, Q_2 and Ω only. Rewriting Eq.A 5.32 in term of I_{1max} gives

$$i_1(t) = \underbrace{A_1\, e^{-\alpha_T t} \cos\left(\omega_T t + \frac{3\pi}{2}\right)}_{\text{1st term}} + \underbrace{A_2 \cos(\Omega t + \varphi_2) + A_3\, e^{-\alpha_T t} \cos(\omega_T t + \varphi_3)}_{\text{2nd term}}$$

1st term
contribution from $v_{C1}(t_{-1})$

2nd term
contribution from $v_s(t)$

------ Eq.A 5.35

Where

$$A_1 = \frac{2\, Q_1\, I_{1\max}}{\sqrt{-1 + 4\,(1-k^2)\, Q_1^2}}$$

$$A_2 = \frac{\sqrt{k^4\ Q_1^2 + (1 + k^2\ Q_1\ Q_2)^2}}{\sqrt{k^4 Q_1^2 + 1}} I_{1\max}$$

$$A_3 = 2\ Q_1 \frac{\sqrt{(1-k^2)}\ \sqrt{(k^4 Q_1^2 + (1+k^2 Q_1 Q_2)^2)}}{\sqrt{(k^4 Q_1^2 + 1)}\ \sqrt{(-1+4\ (1-k^2)\ Q_1^2)}}\ e^{\alpha_T \angle I_1 / \Omega}\ I_{1\max}$$

$$\varphi_2 = -\angle I_1 + \angle g_1$$

$$\varphi_3 = -\frac{\omega_T\ \angle I_1}{\Omega} + \angle g_2$$

For reference, the equations for α_T, ω_T, $\angle I_1, \angle g_1$ and $\angle g_2$ are also summarised here

$$\alpha_T = \frac{\Omega}{2\ Q_1\ (1-k^2)} \qquad \omega_T = \Omega\ \frac{\sqrt{4\ (1-k^2)\ Q_1^2\ -1}}{2\ Q_1\ (1-k^2)}$$

$$\angle I_1 = Arc\tan\left(\frac{1}{\frac{1}{k^2 Q_1} + Q_2}\right)$$

$$\angle g_1 = 2\pi - Arc\tan\left(\frac{1}{k^2\ Q_1}\right)$$

$$\angle g_2 = \pi + Arc\tan\left(\frac{-(2-k^2)}{k^2\sqrt{-1+4\ (1-k^2)\ Q_1^2}}\right)$$

A.5.5 Response of v_{CI}(t)

Integrating i_1(t) in Eq.A 5.35 from t = t_1 to t = t obtains the capacitor voltage at as below

$$v_{C1}(t) = v_{C1}(t_{-1}) + \frac{1}{C_1}\int_{t_{-1}}^{t} i_1(x)dx \qquad \text{------ Eq.A 5.36}$$

Where x is a dummy integration variable. If we arbitrarily define t_{-1} to be zero, using $t_{-1} = 0$ in Eq.A 5.36 yields

$$v_{C1}(t) = v_{C1}(t_{-1}) + \frac{1}{C_1}\int_{0}^{t} i_1(x)dx$$

$$= v_{C1}(t_{-1}) + term1 + term2 + term3$$

------ Eq.A 5.37

Where

$$term\,1 = \frac{A_1}{C_1}\left(\frac{\omega_T}{\omega_T^2 + \alpha_T^2} - \frac{e^{-\alpha_T t}\left(\omega_T \cos(\omega_T t) + \alpha_T \sin(\omega_T t)\right)}{\omega_T^2 + \alpha_T^2}\right)$$

$$term2 = -\frac{2A_2}{C_1}\frac{\sin(\varphi_2)}{\Omega}$$

$$term\,3 = \frac{A_3}{C_1}\left(\begin{array}{l} \dfrac{\alpha_T \cos(\varphi_3) - \omega_T \sin(\varphi_3)}{\omega_T^2 + \alpha_T^2} - \\ \dfrac{e^{-\alpha_T t}(\alpha_T \cos(\varphi_3)\cos(\omega_T t) - \omega_T \cos(\omega_T t)\sin(\varphi_3) - \omega_T \cos(\varphi_3)\sin(\omega_T t)}{\omega_T^2 + \alpha_T^2} \\ - \dfrac{\alpha \sin(\varphi_3)\sin(\omega_T t)}{\omega_T^2 + \alpha_T^2} \end{array}\right)$$

Normalising $v_{C1}(t)$ to V_{C1max}:

Eq.A 5.37 is expressed in terms of I_{1max}. In order to compare with the C_1 voltage in the steady-state, it is better for it to be expressed in terms of V_{C1max}. Eq.A 5.1 gives $v_{C1}(t_{-1}) = -V_{C1max}$ and Eq.A 5.2 shows there is the relation $I_{1max} = \Omega\, C_1\, V_{C1max}$, so Eq.A 5.37 becomes

$v_{C1}(t) = -V_{C1max} + \Omega C_1 \, (term1 + term2 + term3) \, V_{C1max}$

------ Eq.A 5.38

A.5.6 Response of i_2(t)

The response of i_2(t) can be found from that of i_1(t). Firstly, assuming the 3rd term in Eq.A 5.16 does not exist, so Eq.A 5.16 becomes

$$I_2'(s) = \frac{\dfrac{-k}{(1-k^2)\sqrt{L_1 L_2}} v_{C1}(t_{-1})}{s^2 + \dfrac{\Omega s}{(1-k^2)\, Q_1} + \dfrac{\Omega^2}{1-k^2}} + \frac{\dfrac{k\, s}{(1-k^2)\sqrt{L_1 L_2}} V_s(s)}{s^2 + \dfrac{\Omega s}{(1-k^2)\, Q_1} + \dfrac{\Omega^2}{1-k^2}}$$

------ Eq.A 5.39

Eq.A 5.15 and Eq.A 5.39 are identical in form, the only difference is with the coefficients. If we let $coeff_1$ represent the coefficient of I_1(s), then $coeff_1 = \dfrac{C_1 \Omega^2}{1-k^2}$. Let $coeff_2$ represent the coefficient of I_2'(s), there is $coeff_2 = \dfrac{k}{(1-k^2)\sqrt{L_1 L_2}}$, I_2'(s) can be expressed as

$$I_2'(s) = \frac{coeff_2}{coeff_1} I_1(s)$$

$$= \frac{k}{C_1 \Omega^2 \sqrt{L_1 L_2}} I_1(s)$$

$$= k\sqrt{\frac{C_2}{C_1}}\, I_1(s) \qquad \text{------ Eq.A 5.40}$$

Eq.A 5.40 shows I_2'(s) is a scaled I_1(s). According to the Laplace transform linearity property (Appendix 5), the corresponding time-domain responses of I_2'(s) is also a $k\sqrt{\dfrac{C_2}{C_1}}$ scaled i_1(t).

Now consider the 3rd term in Eq.A 5.16. It actually represents the constant $i_2(t_{-1})$ in the s-domain. Therefore, the total $i_2(t)$ is a scaled $i_1(t)$ plus a constant

$$i_2(t) = k\sqrt{\frac{C_2}{C_1}}\, i_1(t) + i_2(t_{-1}) \qquad \text{------ Eq.A 5.41}$$

Converting Eq.A 5.3 in following form

$$I_{1\max} = k\sqrt{\frac{C_1}{C_2}}\frac{1}{\sqrt{1+Q_2^2}} I_{2\max} \qquad \text{------ Eq.A 5.42}$$

Substituting Eq.A 5.3, Eq.A 5.42 and Eq.A 5.35 into Eq.A 5.41, obtains $i_2(t)$ which is represented in terms of I_{2max} as following

$$i_2(t) = B_1\, e^{-\alpha_T t}\cos\left(\omega_T\, t + \frac{3\pi}{2}\right) + B_2\cos(\Omega t + \varphi_2) + B_3\, e^{-\alpha_T t}\cos(\omega_T\, t + \varphi_3) + B_4$$

AC term ↓ DC term

------ Eq.A 5.43

Where

$$B_1 = \frac{2\, Q_1\, I_{2\max}}{\sqrt{1+Q_2^2}\,\sqrt{-1+4\,(1-k^2)\,Q_1^2}}$$

$$B_2 = \frac{\sqrt{(1+k^2 Q_1 Q_2)^2 + k^4 Q_1^2}}{\sqrt{1+Q_2^2}\,\sqrt{1+k^4\,Q_1^2}} I_{2\max}$$

$$B_3 = \frac{2Q_1\sqrt{1-k^2}\,\sqrt{(1+k^2 Q_1 Q_2)^2 + k^4 Q_1^2}}{\sqrt{1+Q_2^2}\,\sqrt{1+k^4\,Q_1^2}\,\sqrt{-1+4(1-k^2)Q_1^2}}\, e^{\alpha_T \angle I_1/\Omega}\, I_{2\max}$$

$$B_4 = \frac{Q_2}{\sqrt{1+Q_2^2}} I_{2\max}$$

$$\varphi_2 = -\angle I_1 + \angle g_1$$

$$\varphi_3 = -\frac{\omega_T \angle I_1}{\Omega} + \angle g_2$$

To summarise the first section, the mathematic formulae of $i_1(t)$, $v_{C1}(t)$ and $i_2(t)$ for stage 2 ($t_{-1} < t \leq t_0$) have been derived, represented by Eq.A 5.35, Eq.A 5.38 and Eq.A 5.43 respectively.

A.5.7 Test the hypothesis

The hypothesis states three points: first, because stage 2 is brief, the current and voltage in the primary circuit are not much affected by the switching action during the period, they behave as though they are still in the steady-state; second, in the secondary circuit, the significant effect of switching is that it holds the current $i_2(t)$ at the level of $i_2(t_{-1})$. By the time of $t = t_0$, it is as if the phase of $i_2(t)$ is inverted; finally, if the previous two assumptions are true, the values of $i_1(t_0)$, $v_{C1}(t_0)$ and $i_2(t_0)$ can be simply estimated from the steady-state response. From Eq. 4.13, Eq. 4.14, Eq. 4.15 and Eq. 4.16 in Section 4.3, Chapter 4, there would be

$$\left.\begin{aligned} & i_1(t_0) \approx 0 \\ & v_{C1}(t_0) \approx V_{C1max} \\ & i_2(t_0) \approx I_{2\,max} \sin(\angle I_2 - \angle I_1) \\ & v_{C2}(t_0) = 0 \end{aligned}\right\} \quad \text{------ Eq.A 5.44}$$

The points will be tested by comparing the derived $i_1(t)$, $v_{C1}(t)$, $i_2(t)$ for stage 2 to the corresponding signals if they were in steady-state in the same period.

A.5.7.1 Comparing $i_1(t)$

The i_1(t) for stage 2 is denoted by Eq.A 5.35, i_1(t) for the steady-state is by Eq.A 5.9. Their expressions are very different. However, Eq.A 5.35 is made of two parts: the 1st part is the response when the C_1 discharges from $v_{C1}(t_{-1})$, it is a decaying cosine wave; The 2nd part is the response by the external force v_s(t), it is an increasing cosine wave. Fig A.5. 1 plots an illustration of the two terms.

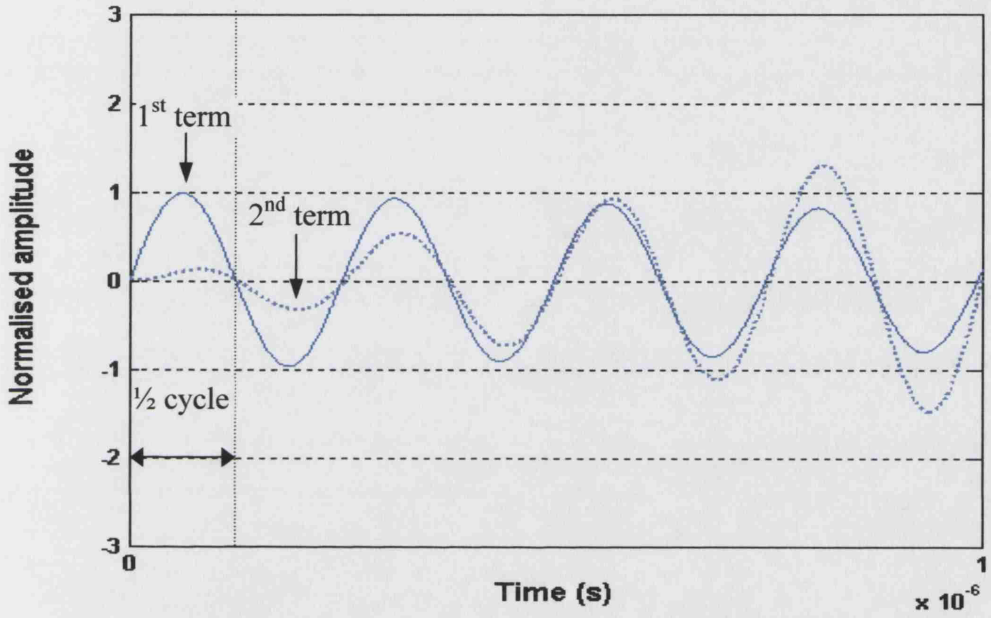


Fig A.5. 1 The 1st term and the 2nd term of i_1*(t) for stage 2*

Because stage 2 lasts only half a cycle, the 1st part is greater than the 2nd part during this period, so it is the dominant factor. Rewriting the 1st part of i_1(t) as below

$$1^{st}\ part\ of\ i_1(t)\ in\ stage\ 2 = A_1\, e^{-\alpha_T t} \cos\left(\omega_T t + \frac{3\pi}{2}\right) \qquad \text{------ Eq.A 5.45}$$

In Chapter 2, we have defined the working range of k, Q_1 and Q_2, they are $30 \le Q_1 \le 100$, $10 \le Q_2 \le 30$, $0.01 \le k \le 0.16$. When the k, Q_1 and Q_2 are within the working range, $A_1\, e^{-\alpha t}$ in Eq.A 5.45 is comparable to I_{1max}, ω is comparable to Ω. Hence Eq.A 5.45 is comparable to Eq.A 5.9 as long as the time is short. Fig A.5. 2 is an example demonstrating their comparability. It plots the 1st part of i_1(t) for stage 2 at the

top of the working range (Q_1 = 100, Q_2 = 30, k = 0.16), and i_1(t) for the steady-state. Both have f_0 = 4 MHz.

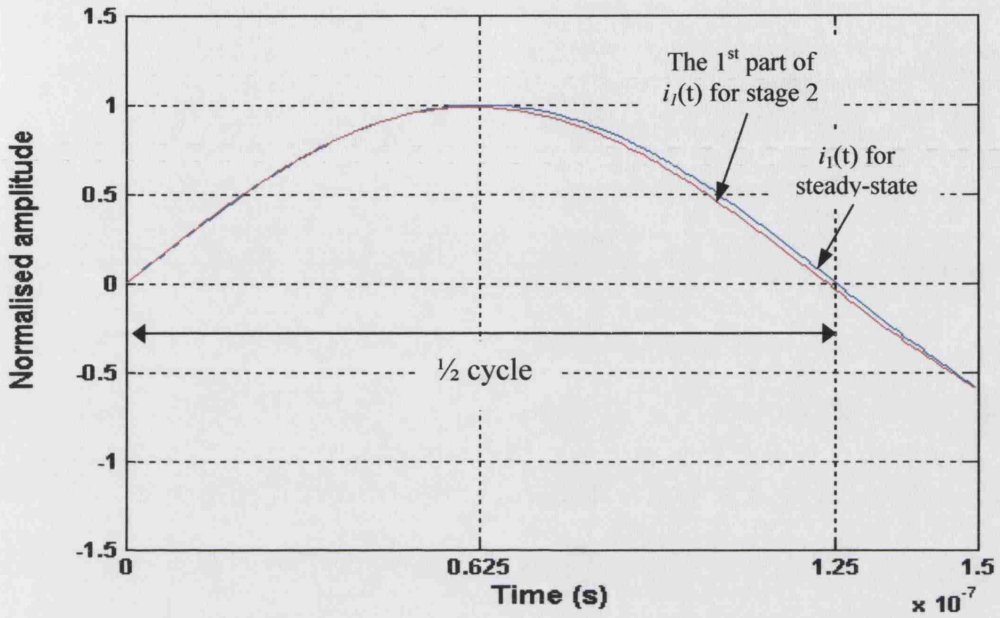


Fig A.5. 2 Comparing the 1st part of i_1*(t) in stage 2 to* i_1*(t) in the steady-state, at* Q_1 = 100, Q_2 = 30 k = 0.16, f_0 = 4 MHz.

Now examining the significance of the 2nd part during the period of stage 2. Rewriting the 2nd part of i_1(t) as below, in which A_2, A_3, α_T, ω_T, φ_2 and φ_2 are the functions of k, Q_1 and Q_2.

$$2^{nd} \text{ part of } i_1(t) \text{ in stage } 2 = A_2 \cos(\Omega t + \varphi_2) + A_3\, e^{-\alpha_T t} \cos(\omega_T t + \varphi_3)$$

------ Eq.A 5.46

Fixing the values of Q_2 and k, plot the 2nd part versus t at various Q_1 in Fig A.5. 3. It shows the 2nd part of i_1(t) does not changes significantly with Q_1.

Fixing the value of Q_1, let k = 0.04, plot the 2nd part versus t at various Q_2 in Fig A.5. 4 A; let k = 0.1, plot the 2nd part versus t at various Q_2 in B; let k = 0.16, plot the 2nd part versus t at various Q_2 in C.

Fig A.5. 4 demonstrates that at a smaller k, the 2nd part of i_1(t) is small, is trivial compared with the 1st part (see Fig A.5. 2); but when k gets greater, it becomes significantly large and should not be ignored. The value of Q_2 has much more effect when k is larger.

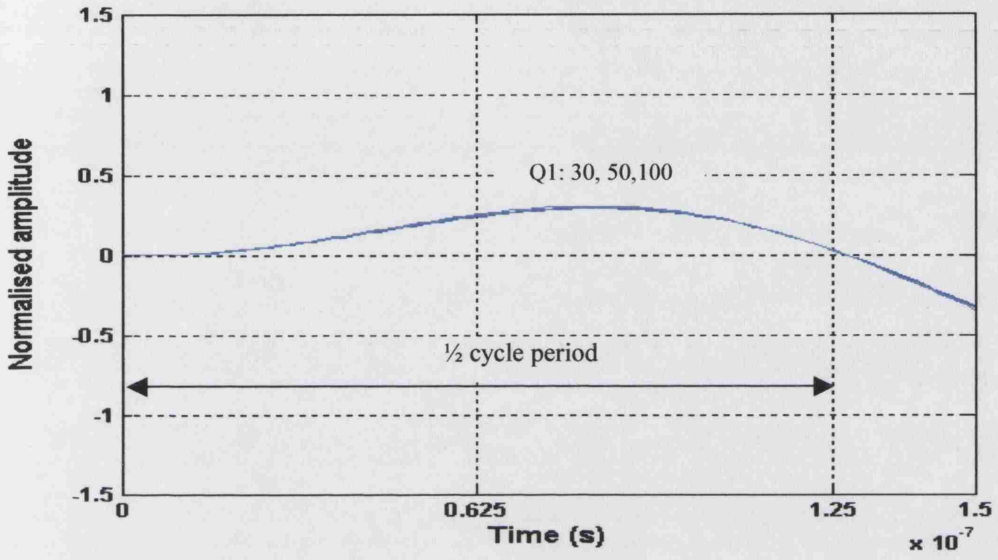


Fig A.5. 3 The 2nd part of i_1(t) in stage 2 at different values of Q_1, when k = 0.16, Q_2 = 12, f_0 = 4 MHz.

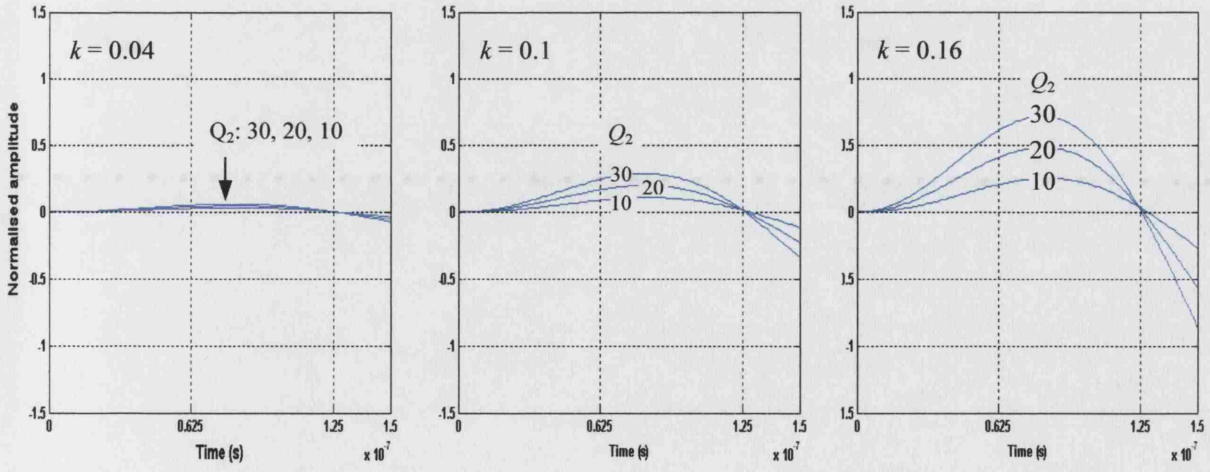


Fig A.5. 4 The 2nd part of i_1(t) in stage 2 at different Q_2 and k, when Q_1 =52, f_0 = 4 MHz.

Therefore, when the coupling is weak the i_1(t) for stage 2 can be represented by the 1st part only, which resembles to the i_1(t) for the steady-state; but when coupling is greater, it is greater than the steady-state i_1(t). Similar conclusion can be expected for the v_{C1}(t) in stage 2.

So the first point of the hypothesis is only true for the weaker coupling.

A.5.7.2 Comparing i_2(t)

The expression for i_2(t) in stage 2 is represented by Eq.A 5.43, it consists of an AC term and a DC term. The AC term resembles to the expression of i_1(t) in stage 2 except the amplitude A_1, A_2 and A_3 in i_1(t) is scaled down to B_1, B_2 and B_3 in i_2(t). Thus one could expect it has similar response with smaller amplitude. The DC term equals $i_2(t_1)$. The AC term is the influence of the primary circuit and the DC term is the effect of shorting the two terminals. How significant is the AC term compared to the DC term? Fig A.5. 5 plots the response of i_2(t) at the top of the working range (k = 0.16, Q_1 = 100, Q_2 = 30) and the DC term. It shows the DC term is the dominant factor.

So the second point of hypothesis is true.

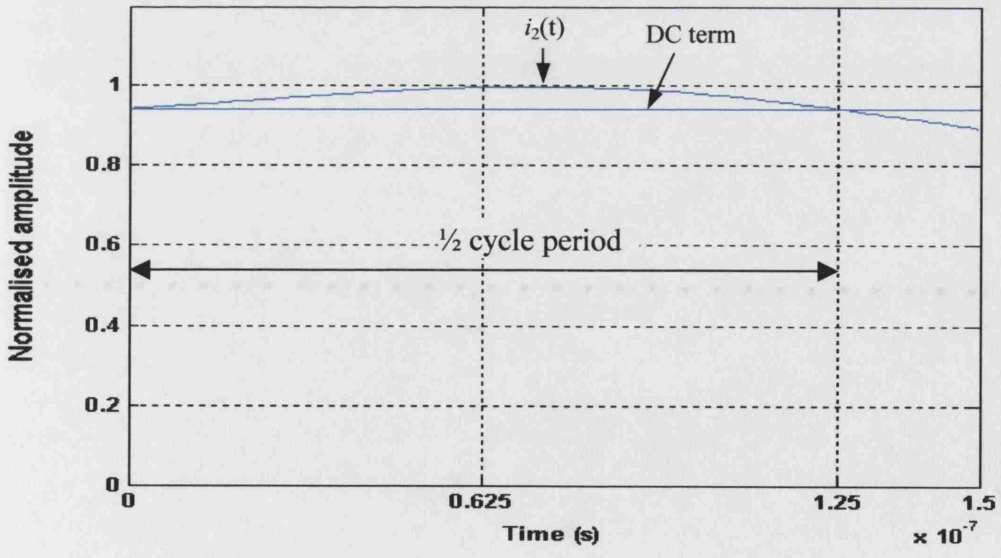


Fig A.5. 5 Comparing i_2*(t) and the DC term of* i_2*(t) in stage 2, at* k = 0.16, Q_1 = 100, Q_2 = 30, f_0 = 4MHz.

A.5.7.3 The signal values

In the hypothesis we were hoping to be able to estimate the signal values for $t = t_0$ from known steady-state response, which is a much simpler procedure. Now we have concluded that the hypothesis is only true at the smaller *k*s but not at the larger *k*s. What differences will be made to the signal values? We will examine them next.

1) Determining the value of $i_1(t_0)$

In Fig A.5. 2, the 1st part of $i_1(t)$ returns to approximately 0 at the ½ cycle period point, as does the 2nd part of $i_1(t)$ in Fig A.5. 3 and Fig A.5. 4 no matter what the *k*, Q_1 and Q_2 are. Therefore one would expect that $i_1(t)$ is also approximately 0 at this point, which is $t = t_0 = \pi/\Omega$. To examine the value of $i_1(t_0)$, let $t = t_0 = \pi/\Omega$, choose Q_1 from $30 \leq Q_1 \leq 100$, Q_2 from $10 \leq Q_2 \leq 30$, substitute them into Eq.A 5.35 , plot $\frac{i_1(t_0)}{I_{1\max}}$ versus *k*. Fig A.5. 6 shows the worst case within the working range, in which $\frac{i_1(t_0)}{I_{1\max}}$ has the largest absolute value (at $Q_1 = 30$, $Q_2 = 30$). It demonstrates $i_1(t_0)$ is small compared to $I_{1\max}$, thus there is

$$i_1(t_0) \approx 0$$

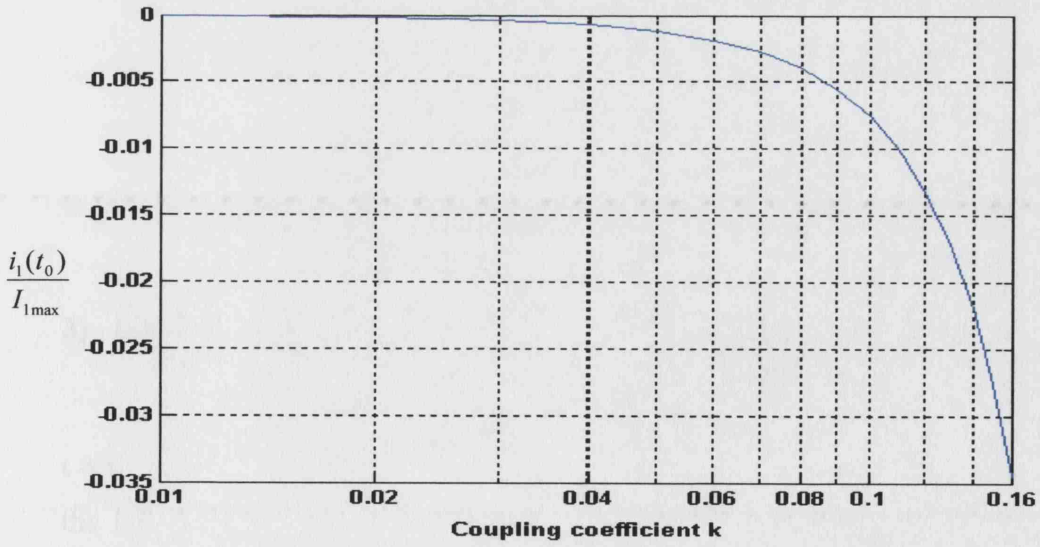


Fig A.5. 6 The value of $i_1(t_0)$ *for worst case at* $Q_1 = 30$, $Q_2 = 30$.

2) Determining the value of $v_{C1}(t_0)$

Let $t = t_0 = \pi/\Omega$, choose Q_1 from $30 \le Q_1 \le 100$, Q_2 from $10 \le Q_2 \le 30$, substitute them into to Eq.A 5.38, plot $\frac{v_{C1}(t_0)}{V_{C1\max}}$ versus k. Fig A.5. 7 shows the case in which $\frac{v_{C1}(t_0)}{V_{C1\max}}$ is largest (at $Q_1 = 100$, $Q_2 = 30$) and the case in which $\frac{v_{C1}(t_0)}{V_{C1\max}}$ is smallest (at $Q_1 = 30$, $Q_2 = 10$) within the working range. It demonstrates that at the smaller k, $v_{C1}(t_0)$ is close to V_{C1max}; but when the k is larger, $v_{C1}(t_0) > V_{C1max}$.

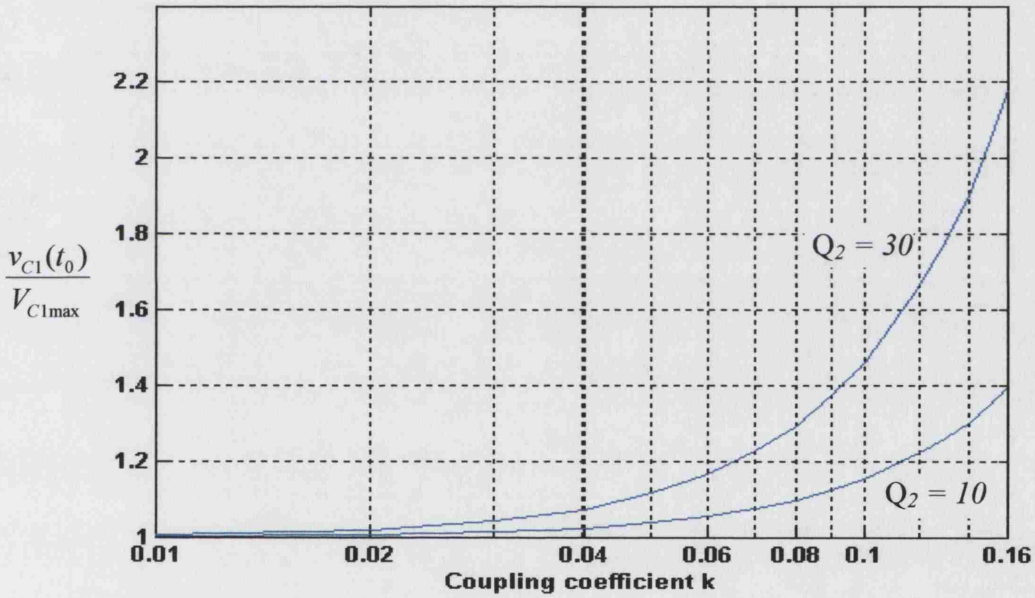


Fig A.5. 7 The largest value of $v_{C1}(t_0)$ (when $Q_1 = 100$, $Q_2 = 30$) and the smallest value of $v_{C1}(t_0)$ (when $Q_1 = 30$, $Q_2 = 10$).

3) Determining the value of $i_2(t_0)$

Because the AC term of $i_2(t)$ in stage 2 is a down-scaled $i_1(t)$, one could expect at $t = t_0$, it closes to 0 so that $i_2(t_0)$ is approximately the DC term. Comparing the $i_2(t_0)$ with the DC term within the working range of k, Q_1 and Q_2 indicates it is true. Fig A.5. 8 illustrates an example in which $t = t_0 = \pi/\Omega$, $Q_1 = 30$ and $Q_2 = 30$ are substituted into

Eq.A 5.43, plot $\frac{i_2(t_0)}{I_{2\max}}$ versus k and $\frac{DC\ term}{I_{2\max}}$ versus k. It shows when the k gets greater, $\frac{i_2(t_0)}{I_{2\max}}$ diverts from $\frac{DC\ term}{I_{2\max}}$, but the difference is small compared to their own values. So there is

$$i_2(t_0) \approx i_2(t_{-1})$$

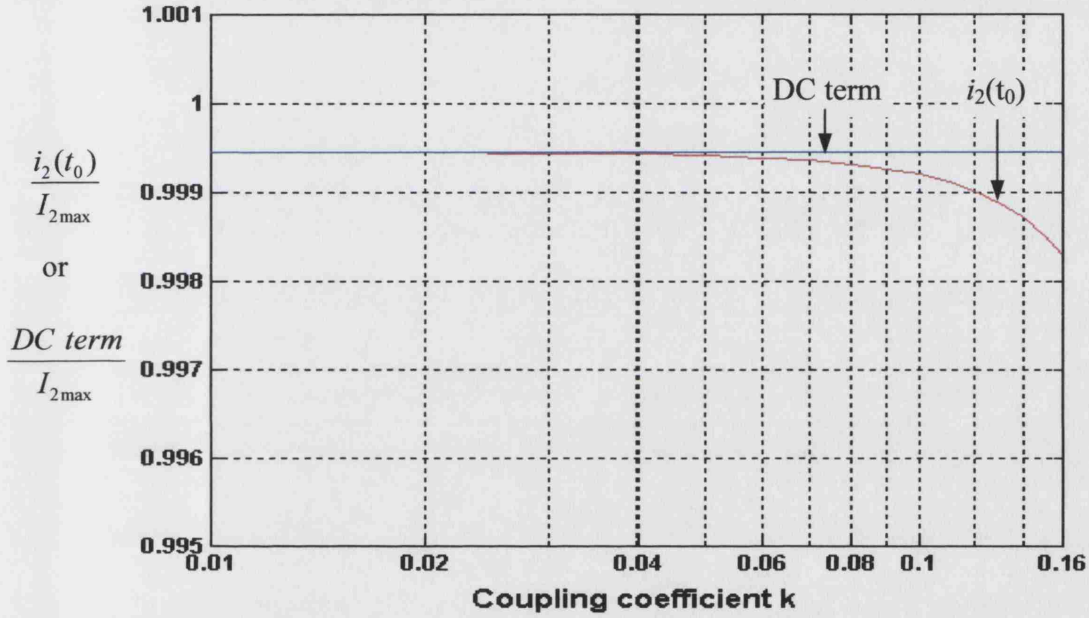


Fig A.5. 8 Comparing $i_2(t_0)$ with its DC term.

4) **The values of $v_{C2}(t_0)$**

Because the switch is closed in this period, the voltage on C_2 is kept at zero, therefore at $t = t_0$

$$v_{C2}(t_0) = 0$$

5) **The value of $v_s(t)$**

The external source will not be affected by the changes of the circuit, so that at $t = t_0$, $v_s(t)$ will have moved forward by a phase of π, giving

$$v_s(t_0) = E\cos(\frac{3\pi}{2} + \pi - \angle I_1)$$

$$= E\cos(2\pi + \frac{\pi}{2} - \angle I_1)$$

------ Eq.A 5.47

Eq.A 5.48 summarise the signal values at t = t_0. Except $v_{C1}(t_0)$, the rest of the signals are similar to the results deduced from the hypothesis in Eq.A 5.44.

$$\left.\begin{array}{ll} i_1(t_0) \approx 0 & \\ v_{C1}(t_0) \approx V_{C1max} & \text{when } k \text{ is small} \\ v_{C1}(t_0) > V_{C1max} & \text{when } k \text{ is large} \\ i_2(t_0) \approx i_2(t_{-1}) = I_{2\,max}\sin(\angle I_1 - \angle I_2) & \\ v_{C2}(t_0) = 0 & \\ v_s(t_{-1}) = E\cos(2\pi + \frac{\pi}{2} - \angle I_1) & \end{array}\right\} \quad \text{------ Eq.A 5.48}$$

A.5.8 Conclusion

A.5.8.1 Conclusion

Two conclusions can be drawn from the above analysis under the condition that the switch closure period is short:

First, at weak coupling, the switch action in the secondary circuit does not significantly affect the primary circuit. i_1 and v_{C1} are nearly the same as they would be in the steady-state situation. The influence of the primary circuit on the secondary current is also trivial. i_2 is dominated by the DC current which results from the switch shorting the two terminals of L_2, so $i_2(t_{-1})$ is held until t = t_0. Therefore the hypothesis stands, the signal values can be estimated from the steady state response.

Second, when the coupling is greater (larger k), the influence that the two circuits on each other is noticeable even for a short period. However, at t = t_0, i_1 almost returns to

zero, so does the AC component of i_2, hence $i_1(t_0)$ and $i_2(t_0)$ values estimated from the steady-state still stand. But the value of $v_{C1}(t_0)$ is greater.

The aim of estimating the signal values at $t = t_0$ is to determine the initial conditions for stage 3. $v_{C1}(t_0)$ represents the amount of energy stored in C_1 at the time of $t = t_0$. This energy will release into the coupled circuit after $t > t_0$ and will contribute to the generation of the modulation response. The response has the characters of duration, waveform shape and amplitude. The duration and waveform shape will determined by the circuit's own properties (Q_1, Q_2 and k) and external driving force v_s. Any release of the energy from the inductors and the capacitors will only contribute to the amplitude. Bearing this in mind, we can still let $v_{C1}(t_0) \approx V_{C1max}$ as the initial condition but knowing we will have the smallest response.

A.5.8.2 Practical situation when $R_{sum} \neq 0$

The above analysis is based on the situation assuming L_2 and the switch are the ideal components. However, in the Section 4.4, Chapter 4, we have discussed that in a practical situation, there are resistances from the inductor L_2 and the switch in series with L_2 during the switch closing period, their sum is denoted as R_{sum}.

R_{sum} consumes energy. During stage 2, the current in L_2 is discharging through it, therefore $i_2(t)$ is decreasing. By the time of $t = t_0$, $i_2(t_0)$ becomes less than the initial value $i_2(t_{-1})$. However, R_{sum} is often small, the discharging can be ignored.

A.5.8.3 Summary

Although testing the hypothesis shows it is not totally true, we are still able to determine the initial conditions for stage 3 from the steady-state response. They are

$i_1(t_0) \approx 0$
$v_{C1}(t_0) \approx V_{C1max}$
$i_2(t_0) \approx i_2(t_{-1}) = I_{2\max} \sin(\angle I_1 - \angle I_2)$
$v_{C2}(t_0) = 0$
$v_s(t_0) = E\cos(2\pi + \frac{\pi}{2} - \angle I_1)$

Appendix 6 Laplace transform of two-terminal passive circuit elements R, L, C with initial conditions [1] and some basic transforms

A6.1 Laplace Linearity property

Lapalce-transform $\{A\, f_1(t) + B\, f_2(t)\} = A\, F_1(s) + B\, F_2(s)$

Inverse-Lapace-transform $\{A F_1(s) + B F_2(s)\} = A\, f_1(t) + B f_2(t)$

A6.2 Laplace differential property

Time-domain differentiation of a waveform *f*(t) is accomplished in s-domain by algebraic process of multiplying the transform F(s) by s and subtracting the constant *f*(0-). Note that the constant *f*(0-) is the value of *f*(t) at t = 0- just prior to t = 0. That is:

$$\text{Laplace transform}\left(\frac{df(t)}{dt}\right) = sF(s) - f(0\_)$$

A6.3 Laplace integration property

Time-domain integration of a waveform *f*(t) is accomplished in the s-domain by algebraic process of dividing the transform F(s) by s.

$$\text{Laplace-transform}\left[\int_0^t f(\tau)\,d\tau\right] = \frac{F(s)}{s}$$

A6.4 The Laplace transform of two-terminal passive circuit elements R, L, C with initial conditions

In time domain their *i-v* relationships are

[1] [98] Page 518, 512, 519, 573.

$$\text{Resistor}: \; v_R(t) = R\, i_R(t)$$

$$\text{Inductor}: \; v_L(t) = L\frac{di_L(t)}{dt}$$

$$\text{Capacitor}: \; v_C(t) = \frac{1}{C}\int_0^t i_C(\tau)\,d\tau + v_C(0)$$

Laplace transform of both side of each equation using the linearity, differentiation, and integration properties.

$$\text{Resistor}: \; V_R(s) = R\, I_R(s)$$

$$\text{Inductor}: \; V_L(s) = Ls\, I_L(s) - L i_L(0)$$

$$\text{Capacitor}: \; V_C(s) = \frac{1}{Cs} I_C(s) + \frac{V_C(0)}{s}$$

A6.5 Some basic transforms

Signal	Waveform f(t), t > 0	Transform F(s)
Impulse	δ(t)	1
Step fuction	u(t)	$\frac{1}{s}$
Ramp	t	$\frac{1}{s^2}$
Exponential	$e^{-\alpha t}$	$\frac{1}{s+\alpha}$
Damped ramp	$te^{-\alpha t}$	$\frac{1}{(s+\alpha)^2}$
Sine	sin(αt)	$\frac{\beta}{s^2+\beta^2}$
Cosine	cos(βt)	$\frac{s}{s^2+\beta^2}$
Damped sine	$e^{-\alpha t}\sin(\beta t)$	$\frac{\beta}{(s+\alpha)^2+\beta^2}$

Damped cosine	$e^{-\alpha t}\cos(\beta t)$	$\frac{s+\alpha}{(s+\alpha)^2+\beta^2}$

Appendix 7 Deriving analytical solution of the natural response of the primary current with the initial condition $i_2(t_0) = 2I_{2max}$

A.7.1 Introduction

This appendix is to derive analytical expression for natural response of the primary current in stage 3. The equation manipulation procedure will follow that described in Pierce's book [81]. However, the problem being solved here is for a circuit configuration different from Pierce's. In this appendix the primary circuit is series tuned and the secondary circuit is parallel tuned while in Pierce's study the secondary is series tuned.

There are three reasons to conduct the study: firstly, in searching the literature the author has not found the analytical solution of transient response for the circuit configuration concerned here. Therefore it is a contribution to existing knowledge; secondly, it is an alternative to the method the author has developed in Chapter 4 and Chapter 5. Two methods can be compared or used to support for each other; thirdly, the equation manipulation procedure developed by Pierce and the others before 1920's might not be well-known to modern time researchers, however the author found it is interesting and wish to share them with the readers.

The procedure is based on classical method. For tutorial, see Pierce's book [81], or Guillemin's book [43], etc.

The problem is to find the natural response of $i_{1natural}(t)$, denoted by $i_1(t)$ in this appendix for simplicity, in stage 3. The initial condition is $i_2(t_0) \approx 2\ I_{2max}$.

A.7.2 General solution

Rewriting Eq. 4.29, Chapter 4, the differential equations describing natural response of the circuit are:

$$\left.\begin{aligned} & R_1 i_1 + L_1 \frac{di_1}{dt} + \frac{1}{C_1}\int i_1 dt - M\frac{di_2}{dt} = 0 \\ & -M\frac{di_1}{dt} + L_2\frac{di_2}{dt} + \frac{1}{C_2}(\int i_2 dt - \int i_3 dt) = 0 \\ & \frac{1}{C_2}(\int i_3 dt - \int i_2 dt) + R_2 i_3 = 0 \end{aligned}\right\} \quad \text{------ Eq.A 7.1}$$

Eq.A 7.1 contains three linear homogeneous differential equations. In exponential form, the general solutions for such equations are

$$i_1 = Ae^{st},\ i_2 = Be^{st},\ i_3 = Ce^{st} \quad \text{------ Eq.A 7.2}$$

In which s, A, B and C are constants to be determined. For solving the natural response of $i_1(t)$, only s and A are to needed. In following sections they will be dealt with separately.

Note that from Eq.A 7.2, the following relations can be derived:

$$\frac{di_1}{dt} = Ase^{st},\ \frac{di_2}{dt} = Bse^{st} \quad \text{------ Eq.A 7.3}$$

$$\int i_1 dt = \frac{Ae^{st}}{s},\ \int i_2 dt = \frac{Be^{st}}{s},\ \int i_3 dt = \frac{Ce^{st}}{s} \quad \text{------ Eq.A 7.4}$$

A.7.3 Determining s

A.7.3.1 Characteristic equation

1) Characteristic equation

Substituting Eq.A 7.2, Eq.A 7.3, Eq.A 7.4 into Eq.A 7.1, cancel e^{st}, gives

$$\left.\begin{aligned} R_1 A + L_1 As + \frac{A}{c_1 s} - M Bs = 0 \\ -MAs + L_2 Bs + \frac{B}{sc_2} - \frac{C}{sc_2} = 0 \\ \frac{C}{sc_2} - \frac{B}{sc_2} + R_2 C = 0 \end{aligned}\right\} \quad \text{------ Eq.A 7.5}$$

Cancelling A, B and C, gives

$$C_1C_2(L_1L_2 - M^2)s^4 + C_1(L_1L_2 - M^2 + C_2L_2R_1R_2)s^3 + (C_1L_2R_1 + C_1L_1R_2 + C_2L_2R_2)s^2$$

$$+ (L_2 + C_1R_1R_2)s + R_2 = 0$$

------ Eq.A 7.6

Eq.A 7.6 is the circuit characteristic equation because its roots determine the signal attributes.

2) Characteristic equation expressed by Ω_1, Ω_2, α_1 and α_2

We know k is the coupling coefficient, and there is

$$M = k\sqrt{L_1L_2} \quad \text{------ Eq.A 7.7}$$

Letting Ω_1 and Ω_2 be resonant frequency of the primary and secondary circuits respectively when each is alone, there are

$$\Omega_1 = \sqrt{\frac{1}{L_1 C_1}}, \quad \Omega_2 = \sqrt{\frac{1}{L_2 C_2}} \qquad \text{------ Eq.A 7.8}$$

Letting α_1, α_2 be damping constants of the primary and secondary circuits when each is alone and uninfluenced by the other, there are

$$a_1 = \frac{R_1}{2L_1}, \quad a_2 = \frac{1}{2R_2 C_2} \qquad \text{------ Eq.A 7.9}$$

Bringing Eq.A 7.7, Eq.A 7.8 and Eq.A 7.9 into Eq.A 7.6, we have

$$s^4 + \frac{2(a_1 + a_2 - a_2 k^2)}{1-k^2} s^3 + \frac{\Omega_1^2 + \Omega_2^2 + 4a_1 a_2}{1-k^2} s^2 + \frac{2(a_1 \Omega_2^2 + a_2 \Omega_1^2)}{1-k^2} s + \frac{\Omega_1^2 \Omega_2^2}{1-k^2} = 0$$

------Eq.A 7.10

3) Characteristic equation expressed by a', a'', ω' and ω''

Eq.A 7.10 is a fourth order polynomial equation of s. Hence, it has four roots, written in the complex forms they are

$$\left.\begin{aligned} s_1 &= -\alpha' + j\omega' \\ s_2 &= -\alpha' - j\omega' \\ s_3 &= -\alpha'' + j\omega'' \\ s_4 &= -\alpha'' - j\omega'' \end{aligned}\right\} \qquad \text{------Eq.A 7.11}$$

In which α' and α" are always real, ω' and ω'' can be real resulting in complex roots, or imaginary resulting in real roots.

Representing Eq.A 7.10 by roots s_1, s_2, s_3 and s_4, gives

$$(s-s_1)(s-s_2)(s-s_3)(s-s_4)=0 \qquad \text{------Eq.A 7.12}$$

Bringing Eq.A 7.11 into Eq.A 7.12, expending the equation and collecting coefficients according to the order of s, result in

$$(s+\alpha'-j\omega')(s+\alpha'+j\omega')(s+\alpha''-j\omega'')(s+\alpha''+j\omega'')$$

$$=s^4+2(\alpha'+\alpha'')s^3+(\alpha'^2+4\alpha'\alpha''+\alpha''^2+\omega'^2+\omega''^2)s^2+2(\alpha'^2\alpha''+\alpha'\alpha''^2+\alpha''\omega'^2+\alpha'\omega''^2)s$$
$$+(\alpha'^2\alpha''^2+\alpha''^2\omega'^2+\alpha'^2\omega''^2+\omega'^2\omega''^2)$$
$$=0$$

------Eq.A 7.13

Letting

$$\Omega'^2=a'^2+\omega'^2$$
$$\Omega''^2=a''^2+\omega''^2$$

Eq.A 7.13 becomes

$$s^4+2(a'+a'')s^3+(\Omega'^2+\Omega''^2+4a'a'')s^2+2(a'\Omega''^2+a''\Omega'^2)s+\Omega'^2\Omega''^2=0$$

------Eq.A 7.14

A.7.3.2 Physical meaning of a', a'', ω' and ω''

When each primary or secondary circuit is alone and uninfluenced by the other, each circuit oscillates at a natural frequency, ω_1 for the primary circuit and ω_2 for the secondary circuit. There are relations

$$\omega_1^2 = \Omega_1^2 - \alpha_1^2$$

$$\omega_2^2 = \Omega_2^2 - \alpha_2^2$$

Ω_1, Ω_2 are resonant frequencies, α_1 and α_2 are damping constants. They are denoted by component values in the corresponding circuit.

When the two circuits are coupled via electrical-magnetic field, there are still two oscillations but shared by both primary and secondary circuits. Currents and voltages in both the primary and secondary circuits are doubly periodic, oscillating at ω' and ω''. Each oscillation has its own damping constants, a' for ω' and a'' for ω'', there are

$$\left.\begin{aligned} \omega'^2 &= \Omega'^2 - a'^2 \\ \omega''^2 &= \Omega''^2 - a''^2 \end{aligned}\right\} \quad \text{-------Eq.A 7.15}$$

Ω' and Ω'', α' and α'' are expected to be denoted by component values from both circuits.

A.7.3.3 Solving a', a'', ω' and ω''

In order to determine four s's in Eq.A 7.11, a', a'', ω' and ω'' have to be solved. Solving a', a'', ω' and ω'' means expressing them in terms of known circuit parameters k, Ω_1, Ω_2, α_1 and α_2.

A.7.3.4 Comparing the coefficients

Comparing the coefficients of Eq.A 7.14 with their counterpart in Eq.A 7.10, gives

$$\alpha' + \alpha'' = \frac{a_1 + a_2 - a_2 k^2}{1 - k^2} \quad \text{------Eq.A 7.16}$$

$$\Omega'^2 + \Omega''^2 + 4\alpha'\alpha'' = \frac{\Omega_1^2 + \Omega_2^2 + 4a_1 a_2}{1 - k^2} \quad \text{------Eq.A 7.17}$$

$$\alpha' \Omega''^2 + \alpha'' \Omega'^2 = \frac{2(a_1 \Omega_2^2 + a_2 \Omega_1^2)}{1 - k^2} \quad \text{------Eq.A 7.18}$$

$$\Omega'^2 \Omega''^2 = \frac{\Omega_1^2 \Omega_2^2}{1 - k^2} \quad \text{------Eq.A 7.19}$$

Letting Eq.A 7.16 be divided by Eq.A 7.19 obtains

$$\frac{\alpha' + \alpha''}{\Omega'^2 \Omega''^2} = \frac{a_1 + a_2 - a_2 k^2}{\Omega_1^2 \Omega_2^2} \quad \text{-------Eq.A 7.20}$$

Letting Eq.A 7.17 be divided by Eq.A 7.19 obtains

$$\frac{1}{\Omega'^2} + \frac{1}{\Omega''^2} = \frac{1}{\Omega_1^2} + \frac{1}{\Omega_2^2} + \frac{z}{\Omega_1 \Omega_2} \quad \text{------Eq.A 7.21}$$

Where

$$z = \frac{4(a_1 a_2 - (1 - k^2)a'a'')}{\Omega_1 \Omega_2} \quad \text{------Eq.A 7.22}$$

Letting Eq.A 7.18 be divided by Eq.A 7.19 obtains

$$\frac{a'}{\Omega'^2}+\frac{a''}{\Omega''^2}=\frac{a_1}{\Omega_1^2}+\frac{a_2}{\Omega_2^2}$$ ------Eq.A 7.23

Converting Eq.A 7.19 to

$$\frac{1}{\Omega'\Omega''}=\frac{\sqrt{1-k^2}}{\Omega_1\Omega_2}$$ ------Eq.A 7.24

1) Finding Ω', Ω''

Making Sqrt (Eq.A 7.21) + 2 × (Eq.A 7.24), gives

$$\frac{1}{\Omega'}+\frac{1}{\Omega''}=\sqrt{\frac{1}{\Omega_1^2}+\frac{1}{\Omega_2^2}+\frac{1}{\Omega_1\Omega_2}(z+2\sqrt{1-k^2})}$$ ------Eq.A 7.25

Making Sqrt (Eq.A 7.21) - 2 × (Eq.A 7.24), and letting $\Omega' > \Omega''$, gives

$$\frac{1}{\Omega'}-\frac{1}{\Omega''}=\sqrt{\frac{1}{\Omega_1^2}+\frac{1}{\Omega_2^2}+\frac{1}{\Omega_1\Omega_2}(z-2\sqrt{1-k^2})}$$ ------Eq.A 7.26

Making (Eq.A 7.25 + Eq.A 7.26)/2, gives

$$\frac{1}{\Omega'}=\frac{1}{2}\left(\sqrt{\frac{1}{\Omega_1^2}+\frac{1}{\Omega_2^2}+\frac{1}{\Omega_1\Omega_2}(z+2\sqrt{1-k^2})}+\sqrt{\frac{1}{\Omega_1^2}+\frac{1}{\Omega_2^2}+\frac{1}{\Omega_1\Omega_2}(z-2\sqrt{1-k^2})}\right)$$

------Eq.A 7.27

Making (Eq.A 7.25 - Eq.A 7.26)/2, gives

$$\frac{1}{\Omega''}=\frac{1}{2}\left(\sqrt{\frac{1}{\Omega_1^2}+\frac{1}{\Omega_2^2}+\frac{1}{\Omega_1\Omega_2}(z+2\sqrt{1-k^2})}-\sqrt{\frac{1}{\Omega_1^2}+\frac{1}{\Omega_2^2}+\frac{1}{\Omega_1\Omega_2}(z-2\sqrt{1-k^2})}\right)$$

------Eq.A 7.28

2) Finding a', a''

Making (Eq.A 7.23 - Ω'^2 × Eq.A 7.20), then being divided by $(\frac{1}{\Omega'^2}-\frac{1}{\Omega''^2})$ gives

$$a'=\frac{\frac{a_1}{\Omega_1^2}+\frac{a_2}{\Omega_2^2}-(a_1+a_2-a_2k^2)\frac{\Omega'^2}{\Omega_1^2\Omega_2^2}}{\frac{1}{\Omega'^2}-\frac{1}{\Omega''^2}}$$

------Eq.A 7.29

Making (Eq.A 7.23 - Ω''^2 × Eq.A 7.20), then letting it be divided by $(\frac{1}{\Omega'^2}-\frac{1}{\Omega''^2})$ gives

$$a''=-\frac{\frac{a_1}{\Omega_1^2}+\frac{a_2}{\Omega_2^2}-(a_1+a_2-a_2k^2)\frac{\Omega''^2}{\Omega_1^2\Omega_2^2}}{\frac{1}{\Omega'^2}-\frac{1}{\Omega''^2}}$$

------Eq.A 7.30

Ω' can be found by inverting Eq.A 7.27 and Ω'' by inverting Eq.A 7.28. Substituting the values of Ω' and Ω'' into Eq.A 7.29 and Eq.A 7.30, gives

$$a'=\frac{a_1+a_2-a_2k^2}{2(1-k^2)}-\frac{\frac{a_1+a_2-a_2k^2}{2(1-k^2)}(\Omega_1^2+\Omega_2^2+z\Omega_1\Omega_2)-(a_1\Omega_2^2+a_2\Omega_1^2)}{\sqrt{(\Omega_1^2+\Omega_2^2+z\Omega_1\Omega_2)^2-4(1-k^2)\Omega_1^2\Omega_2^2}}$$

------Eq.A 7.31

And

$$a'' = \frac{a_1 + a_2 - a_2 k^2}{2(1-k^2)} + \frac{\frac{a_1 + a_2 - a_2 k^2}{2(1-k^2)}(\Omega_1^2 + \Omega_2^2 + z\Omega_1\Omega_2) - (a_1\Omega_2^2 + a_2\Omega_1^2)}{\sqrt{(\Omega_1^2 + \Omega_2^2 + z\Omega_1\Omega_2)^2 - 4(1-k^2)\Omega_1^2\Omega_2^2}}$$

------ Eq.A 7.32

Eq.A 7.27, Eq.A 7.28, Eq.A 7.31 and Eq.A 7.32 are exact expressions except that z has to be found.

3) Finding *z*

Multiplying a' and a'' from Eq.A 7.31 and Eq.A 7.32, substituting the product into Eq.A 7.22, collecting z in descendent order, we obtain

$$z^3 + cf_1 z^2 + cf_2 z + cf_3 = 0$$ ------ Eq.A 7.33

Where

$$cf_1 = \frac{2(\Omega_1^2 + \Omega_2^2)}{\Omega_1\Omega_2} - \frac{4a_1a_2}{\Omega_1\Omega_2}$$

$$cf_2 = 4k^2 + \frac{(\Omega_1^2 - \Omega_2^2)^2}{\Omega_1^2\Omega_2^2} + \frac{4a_1(a_1 - a_2 - a_2k^2)}{\Omega_1^2} - \frac{4a_2(a_1 - a_2 + a_2k^2)}{\Omega_2^2}$$

$$cf_3 = \frac{4a_1(a_1 - a_2)k^2\Omega_2}{\Omega_1^3} - \frac{4a_2k^2(a_1 - a_2 + a_2k^2)}{\Omega_1\Omega_2}$$

The exact value of z can be found by solving the cubic equation Eq.A 7.33 in Matlab symbolic toolbox. Taking one of the three solutions which has smallest absolute value, that is [1]

$$z = -\frac{1}{3}cf_1 + \frac{1}{6}(36cf_1\,cf_2 - 108cf_3 - 8cf_1^3 + 12\sqrt{12cf_2^3 - 3cf_2^2\,cf_1^2 - 54cf_1\,cf_2\,cf_3 + 81cf_3^2 + 12cf_1^3\,cf_3})^{\frac{1}{3}} - \frac{6*(\frac{1}{3}cf_2 - \frac{1}{9}cf_1^2)}{(36cf_1\,cf_2 - 108cf_3 - 8cf_1^3 + 12\sqrt{12cf_2^3 - 3cf_2^2\,cf_1^2 - 54cf_1\,cf_2\,cf_3 + 81cf_3^2 + 12cf_1^3\,cf_3})^{\frac{1}{3}}}$$

------Eq.A 7.34

4) Summary for *s*

There are four *s*'s. They are expressed in terms of α', α'', ω' and ω'' (Eq.A 7.11). In which α' and α'' are denoted by k, Ω_1, Ω_2, α_1, α_2.and z (Eq.A 7.31 and Eq.A 7.32); ω' and ω'' are denoted by α', α'', Ω' and Ω'' (Eq.A 7.15); Ω' and Ω'' are denoted by k, Ω_1, Ω_2, α_1, α_2.and z (Eq.A 7.27 and Eq.A 7.28); z is by Eq.A 7.34.

In summary, *s*'s are now expressed in terms of known circuit parameters k, Ω_1, Ω_2, α_1 and α_2.

---

[1] Following Pierce's conclusion only.
There is another method to find *z*. According to Pierce, the cubic equation Eq.A 7.33 can be reduced to a quadratic equation over the important range of constants to become

$$cf_1\,z^2 + cf_2\,z + cf_3 = 0 \qquad \text{------Eq. N.1}$$

One of the solutions of Eq. N.1 is the approximate value of z but with sufficient accuracy:

$$z = -\frac{cf_2}{2cf_1}\left(1 - \sqrt{1 - \frac{4cf_1\,cf_3}{cf_2^2}}\right) \qquad \text{------Eq. N.2}$$

For extended investigation, please see Pierce's book [81] p106-108.

A.7.4 Determining *A*

A.7.4.1 Relations among A's, B's and C's.

We have known there are four *s*'s: s_1, s_2, s_3 and s_4. For each *s*, there will be a corresponding *A*, *B* and *C* with same subscripts (one of 1, 2, 3 and 4). One of solutions for i_1 is

$$i_1 = A_n e^{s_n t} \qquad \text{-------Eq.A 7.35}$$

And likewise

$$i_2 = B_n e^{s_n t} \qquad \text{-------Eq.A 7.36}$$

$$i_3 = C_n e^{s_n t} \qquad \text{-------Eq.A 7.37}$$

Where

n = 1, 2, 3, 4

By additivity property of the linear circuit, the complete solutions are

$$\left.\begin{aligned} i_1 &= A_1 e^{s_1 t} + A_2 e^{s_2 t} + A_3 e^{s_3 t} + A_4 e^{s_4 t} = \Sigma A_n e^{s_n t} \\ i_2 &= B_1 e^{s_1 t} + B_2 e^{s_2 t} + B_3 e^{s_3 t} + B_4 e^{s_4 t} = \Sigma B_n e^{s_n t} \\ i_3 &= C_1 e^{s_1 t} + C_2 e^{s_2 t} + C_3 e^{s_3 t} + C_4 e^{s_4 t} = \Sigma C_n e^{s_n t} \end{aligned}\right\} \qquad \text{------Eq.A 7.38}$$

Also there are

$$\left.\begin{aligned}
\frac{di_1}{dt} &= s_1 A_1 e^{s_1 t} + s_2 A_2 e^{s_{21} t} + s_3 A_3 e^{s_3 t} + s_4 A_4 e^{s_4 t} = \sum s_n A_n e^{s_n t} \\
\frac{di_2}{dt} &= s_1 B_1 e^{s_1 t} + s_2 B_2 e^{s_{21} t} + s_3 B_3 e^{s_3 t} + s_4 B_4 e^{s_4 t} = \sum s_n B_n e^{s_n t} \\
\frac{di_3}{dt} &= s_1 C_1 e^{s_1 t} + s_2 C_2 e^{s_{21} t} + s_3 C_3 e^{s_3 t} + s_4 C_4 e^{s_4 t} = \sum s_n C_n e^{s_n t}
\end{aligned}\right\} \quad \text{------Eq.A 7.39}$$

And

$$\left.\begin{aligned}
\int i_1 dt &= \frac{A_1}{s_1} e^{s_1 t} + \frac{A_2}{s_2} e^{s_2 t} + \frac{A_3}{s_3} e^{s_3 t} + \frac{A_4}{s_4} e^{s_{41} t} = \sum \frac{A_n}{s_n} e^{s_n t} \\
\int i_2 dt &= \frac{B_1}{s_1} e^{s_1 t} + \frac{B_2}{s_2} e^{s_2 t} + \frac{B_3}{s_3} e^{s_3 t} + \frac{B_4}{s_4} e^{s_{41} t} = \sum \frac{B_n}{s_n} e^{s_n t} \\
\int i_3 dt &= \frac{C_1}{s_1} e^{s_1 t} + \frac{C_2}{s_2} e^{s_2 t} + \frac{C_3}{s_3} e^{s_3 t} + \frac{C_4}{s_4} e^{s_{41} t} = \sum \frac{C_n}{s_n} e^{s_n t}
\end{aligned}\right\} \quad \text{------Eq.A 7.40}$$

Each individual solution in Eq.A 7.35, Eq.A 7.36 and Eq.A 7.37 satisfies Eq.A 7.1. Substituting each into Eq.A 7.1, cancelling $e^{s_n t}$, gives

$$\left.\begin{aligned}
R_1 A_n + L_1 A_n s_n + \frac{A_n}{C_1 s_n} - M B_n s_n &= 0 \\
-M A_n s_n + L_2 B_n s_n + \frac{B_n}{s_n C_2} - \frac{E_n}{s C_2} &= 0 \\
\frac{E_n}{s_n C_2} - \frac{B_n}{s_n C_2} + R_2 E_n &= 0
\end{aligned}\right\} \quad \text{------Eq.A 7.41}$$

There are four identical Eq.A 7.41's except the subscripts being one of n = 1, 2, 3, and 4. Summing up the four equations, gives

$$\left.\begin{aligned} &R_1\sum A_n + L_1\sum A_n s_n + \frac{1}{C_1}\sum\frac{A_n}{s_n} - M\sum B_n s_n = 0 \\ &-M\sum A_n s_n + L_2\sum B_n s_n + \frac{1}{C_2}\sum\frac{B_n}{s_n} - \frac{1}{C_2}\sum\frac{C_n}{s_n} = 0 \\ &\frac{1}{C_2}\sum\frac{E_n}{s_n} - \frac{1}{C_2}\sum\frac{B_n}{s_n} + R_2\sum C_n = 0 \end{aligned}\right\} \quad \text{------Eq.A 7.42}$$

Dividing each Eq.A 7.41 by corresponding s_n gives another four identical equations. Summing them up, obtains

$$\left.\begin{aligned} &R_1\sum\frac{A_n}{s_n} + L_1\sum A_n + \frac{1}{C_1}\sum\frac{A_n}{s_n^2} - M\sum B_n = 0 \\ &-M\sum A_n + L_2\sum B_n + \frac{1}{C_2}\sum\frac{B_n}{s_n^2} - \frac{1}{C_2}\sum\frac{C_n}{s_n^2} = 0 \\ &\frac{1}{C_2}\sum\frac{C_n}{s_n^2} - \frac{1}{C_2}\sum\frac{B_n}{s_n^2} + R_2\sum\frac{C_n}{s_n} = 0 \end{aligned}\right\} \quad \text{------Eq.A 7.43}$$

Likewise, there are

$$\left.\begin{aligned} &R_1\sum\frac{A_n}{s_n^2}+L_1\sum\frac{A_n}{s_n}+\frac{1}{C_1}\sum\frac{A_n}{s_n^3}-M\sum\frac{B_n}{s_n}=0\\ &-M\sum\frac{A_n}{s_n}+L_2\sum\frac{B_n}{s_n}+\frac{1}{C_2}\sum\frac{B_n}{s_n^3}-\frac{1}{C_2}\sum\frac{C_n}{s_n^3}=0\\ &\frac{1}{C_2}\sum\frac{C_n}{s_n^3}-\frac{1}{C_2}\sum\frac{B_n}{s_n^3}+R_2\sum\frac{C_n}{s_n^2}=0 \end{aligned}\right\}$$ ------Eq.A 7.44

The initial conditions at t = 0 are

$$\left.\begin{aligned} &t=0\\ &i_1(0)=0\\ &i_2(0)=2\,I_{2max},\\ &i_3(0)=0 \end{aligned}\right\}$$ ------Eq.A 7.45

The charges in the capacitor C_1 and C_2 are zero, so

$$\left.\begin{aligned} &q_1(0)=\int i_1\,dt=0\\ &q_2(0)=\int(i_2-i_3)\,dt=0 \end{aligned}\right\}$$ ------Eq.A 7.46

Bringing Eq.A 7.45 into Eq.A 7.38, gives

$$\left.\begin{aligned} &\sum A_n=0\\ &\sum B_n=2I_{2\,max}\\ &\sum C_n=0 \end{aligned}\right\}$$ ------Eq.A 7.47

Bringing Eq.A 7.46 into Eq.A 7.40, gives

$$\left.\begin{aligned}\sum \frac{A_n}{s_n} &= 0 \\ \sum \left(\frac{B_n}{s_n} - \frac{C_n}{s_n}\right) &= 0\end{aligned}\right\} \quad \text{------Eq.A 7.48}$$

Bringing Eq.A 7.47 and Eq.A 7.48 into Eq.A 7.42, obtains

$$L_1 \sum A_n s_n = M \sum B_n s_n$$

$$M \sum A_n s_n = L_2 \sum B_n s_n$$

Solving above equations, gives

$$\sum A_n s_n = 0 \qquad \text{-------Eq.A 7.49}$$

Substituting Eq.A 7.47 and Eq.A 7.48 into Eq.A 7.43, obtain

$$\sum \frac{A_n}{s_n^2} = 2C_1 M I_{2\max} \qquad \text{------Eq.A 7.50}$$

For summary

$$\left.\begin{aligned}
&\sum A_n s_n = 0 \\
&\sum A_n = 0 \\
&\sum \frac{A_n}{s_n} = 0 \\
&\sum \frac{A_n}{s_n^2} = 2C_1 M I_{2\max}
\end{aligned}\right\} \quad \text{-------Eq.A 7.51}$$

A.7.4.2 Solving A_n

Expanding Eq.A 7.51, becomes

$$\left.\begin{aligned}
&A_1 s_1 + A_2 s_2 + A_3 s_3 + A_4 s_4 = 0 \\
&A_1 + A_2 + A_3 + A_4 = 0 \\
&\frac{A_1}{s_1} + \frac{A_2}{s_2} + \frac{A_3}{s_3} + \frac{A_4}{s_4} = 0 \\
&\frac{A_1}{s_1^2} + \frac{A_2}{s_2^2} + \frac{A_3}{s_3^2} + \frac{A_4}{s_4^2} = 2C_1 M I_{2\max}
\end{aligned}\right\} \quad \text{------ Eq.A 7.52}$$

In which A_1, A_2, A_3 and A_4 are unknown parameters. The determinant of Eq.A 7.52 is

$$\Delta = \begin{vmatrix} s_1 & s_2 & s_3 & s_4 \\ 1 & 1 & 1 & 1 \\ \frac{1}{s_1} & \frac{1}{s_2} & \frac{1}{s_3} & \frac{1}{s_4} \\ \frac{1}{s_1^2} & \frac{1}{s_2^2} & \frac{1}{s_3^2} & \frac{1}{s_4^2} \end{vmatrix}$$

A_1 is thus found by Cramer's rule

$$A_1 = \frac{\begin{vmatrix} 0 & s_2 & s_3 & s_4 \\ 0 & 1 & 1 & 1 \\ 0 & \frac{1}{s_2} & \frac{1}{s_3} & \frac{1}{s_4} \\ 2C_1 M I_{2\max} & \frac{1}{s_2^2} & \frac{1}{s_3^2} & \frac{1}{s_4^2} \end{vmatrix}}{\Delta}$$

$$= -\frac{2C_1 I_{2\max} M s_1^2 s_2 s_3 s_4}{(s_1 - s_2)(s_1 - s_3)(s_1 - s_4)}$$

Similarly, there are

$$A_2 = \frac{2C_1 I_{2\max} M s_1 s_2^2 s_3 s_4}{(s_1 - s_2)(s_2 - s_3)(s_2 - s_4)}$$

$$A_3 = -\frac{2C_1 I_{2\max} M s_1 s_2 s_3^2 s_4}{(s_1 - s_3)(s_2 - s_3)(s_3 - s_4)}$$

$$A_4 = \frac{2C_1 I_{2\max} M s_1 s_2 s_3 s_4^2}{(s_1 - s_4)(-s_2 + s_4)(-s_3 + s_4)}$$

Substituting

$s_1 = -\alpha' + j\omega'$, $s_2 = -\alpha' - j\omega'$, $s_3 = -\alpha'' + j\omega''$, $s_4 = -\alpha'' - j\omega''$, $\Omega'^2 = \omega'^2 + a'^2$, $\Omega''^2 = \omega''^2 + a''^2$ into above equations, results in

$$A_1 = \frac{2M C_1 I_{2\max} \Omega'^2 \Omega''^2 (\omega' + j a')}{2\omega'(-a' + a'' + j(\omega' - \omega''))(-a' + a'' + j(\omega' + \omega''))} \quad \text{------ Eq.A 7.53}$$

In Chapter 2, we have a relation between $I_{1\max}$ and $I_{2\max}$ as

$$\frac{I_{2\max}}{I_{1\max}} = \sqrt{\frac{C_2}{C_1}}\, k\sqrt{1+Q_2^2}$$

Substitute this relation into Eq.A 7.53. Let A_1 is denoted in term of I_{1max} rather than I_{2max}. Then write this complex quantity in exponential form, giving

$$A_1 = I_{1\max}\frac{H\Omega'}{2\omega'}e^{j\theta_1}$$

In which

$$H = \frac{\dfrac{2k^2\sqrt{1+Q_2^2}}{\Omega_1\Omega_2}\,\Omega'^2\,\Omega''^2}{\sqrt{((-a'+a'')^2+(\omega'-\omega'')^2)\,((-a'+a'')^2+(\omega'+\omega'')^2)}} \qquad \text{------ Eq.A 7.54}$$

And

$$\theta' = Arc\tan\frac{-(\alpha'^3-2\alpha'^2\alpha''+\alpha'\alpha''^2+\alpha'\omega'^2+\alpha'\omega''^2-2\alpha''\omega'^2)}{\omega'(\alpha'^2-\alpha''^2+\omega'^2-\omega''^2)} \qquad \text{------ Eq.A 7.55}$$

Similarly, we obtain

$$A_2 = I_{1\max}\frac{H\Omega'}{2\omega'}e^{-j\theta'}$$

$$A_3 = I_{1\max}\frac{H\Omega''}{2\omega''}e^{j\theta''}$$

$$A_4 = I_{1\max}\frac{H\Omega''}{2\omega''}e^{-j\theta''}$$

In which

$$\theta'' = Arc\tan\frac{-(\alpha''^3 - 2\alpha'\alpha''^2 + \alpha'^2\alpha'' + \alpha''\omega'^2 + \alpha''\omega''^2 - 2\alpha'\omega''^2)}{-\omega''(\alpha'^2 - \alpha''^2 + \omega'^2 - \omega''^2)} \quad \text{------Eq.A 7.56}$$

A.7.5 Natural response of $i_1(t)$

Substituting A's and s's into

$$i_1 = A_1 e^{s_1 t} + A_2 e^{s_2 t} + A_3 e^{s_3 t} + A_4 e^{s_4 t}$$

i_1 becomes

$$i_1 = \frac{H\Omega'}{\omega'}e^{-\alpha' t}\left(\frac{e^{j(\omega' t+\theta')} + e^{-j(\omega' t+\theta')}}{2}\right) + \frac{H\Omega''}{\omega''}e^{-\alpha'' t}\left(\frac{e^{j(\omega'' t+\theta'')} + e^{-j(\omega'' t+\theta'')}}{2}\right)$$

Written in trigonometric form

$$i_1 = \frac{H\Omega'}{\omega'}e^{-\alpha' t}\cos(\omega' t+\theta') + \frac{H\Omega''}{\omega''}e^{-\alpha'' t}\cos(\omega'' t+\theta'') \quad \text{------Eq.A 7.57}$$

In which H is denoted by Eq.A 7.54, θ' by Eq.A 7.55, θ'' by Eq.A 7.56, ω', ω'' by Eq.A 7.15, α', α'' by Eq.A 7.31 and Eq.A 7.32, Ω', Ω'' by Eq.A 7.27 and Eq.A 7.28.

Eq.A 7.57 is the analytical expression of the natural response of $i_1(t)$ in stage 3 when the initial condition is $i_2(t_0) = 2\,I_{2\max}$. It is the sum of two damped cosine functions. If arbitrarily let $I_{1\max} = 1$, $i_1(t)$ is expressed in terms of known circuit parameters k, Q_2, Ω_1, Ω_2, α_1 and α_2.

As we known the quality factor for the primary circuit alone is

$$Q_1 = \frac{\Omega_1 L_1}{R_1}$$

For secondary circuit is

$$Q_2 = \Omega_2 R_2 C_2$$

So damping factors can be expressed by frequency and quality factor,

$$\alpha_1 = \frac{R_1}{2L_1} = \frac{\Omega_1}{2Q_1} \qquad \text{-------Eq.A 7.58}$$

And

$$a_2 = \frac{1}{2R_2C_2} = \frac{\Omega_2}{2Q_2} \qquad \text{-------Eq.A 7.59}$$

Therefore, $i_1(t)$ is then represented by Ω_1, Ω_2, Q_1, Q_2 and k only.

A.7.6 Verifying the derived solution

The numerical example in Chapter 5 is used here to verify the result. The circuit parameters given in the example are

$Q_1 = 53$

$Q_2 = 12$

$f_1 = f_2 = f_0 = 4$ MHz,

$\Omega_1 = \Omega_2 = 2\pi f_0$

$0.01 \leq k \leq 0.16$

Substituting them into Eq.A 7.58, Eq.A 7.59, Eq.A 7.31, Eq.A 7.32 and Eq.A 7.34, the time constants $1/\alpha'$ and $1/\alpha''$ versus k can be plotted.

Substituting them into Eq.A 7.58, Eq.A 7.59, Eq.A 7.27, Eq.A 7.28 and Eq.A 7.34, and Eq.A 7.15, letting $f_d' = \omega'/2\pi$ and $f_d'' = \omega''/2\pi$, frequencies f_d' and f_d'' versus k can be plotted.

Substituting them into Eq.A 7.58, Eq.A 7.59, Eq.A 7.31, Eq.A 7.32, Eq.A 7.27, Eq.A 7.28, Eq.A 7.34, Eq.A 7.15 and Eq.A 7.54, half of the amplitudes of the two damped sine functions in Eq.A 7.57, $Amp' = \frac{1}{2}\frac{H\Omega'}{\omega'}$ and $Amp'' = \frac{1}{2}\frac{H\Omega''}{\omega''}$ versus k can be plotted.

Similarly, from Eq.A 7.55 and Eq.A 7.56, phase angles θ' and θ'' versus k can be plotted.

Fig.A 7.1 illustrates these results. In Chapter 5, we have substituted the circuit parameters into the transfer function of $I_1(s)$; partial-fraction-expanded the numerical function in Matlab; found $1/\alpha'$, $1/\alpha''$, f_d', f_d'', r', r'', θ' and θ'' and plotted them in Fig. 5.1. Fig.A 7.1 and Fig. 5.1 show the two approaches gain the same result. It demonstrates the analytical solution of natural response of $i_1(t)$ is correct.

A.7.7 Summary

The analytical function of the natural response of $i_1(t)$ is found following Pierce's equation manipulation procedure. The result is exact, and no approximation is made.

The procedure is very ingenious but also complicated. The result is a very large equation. It is for the inductively coupled circuits with the series-tuned primary, parallel-tuned secondary configuration. It is the complimentary to Pierce's result which is for the series-tuned primary, series-tuned secondary configuration.

The equation gives a complete view of $i_1(t)$, it contributes to the existing knowledge on the inductive coupling problem, and is useful for further investigations. However, for understanding the waveform during the modulation, in the author's opinion, the method, which the author has developed in Chapter 4 and Chapter 5, links to the physical phenomena more straightforwardly, and much simpler.

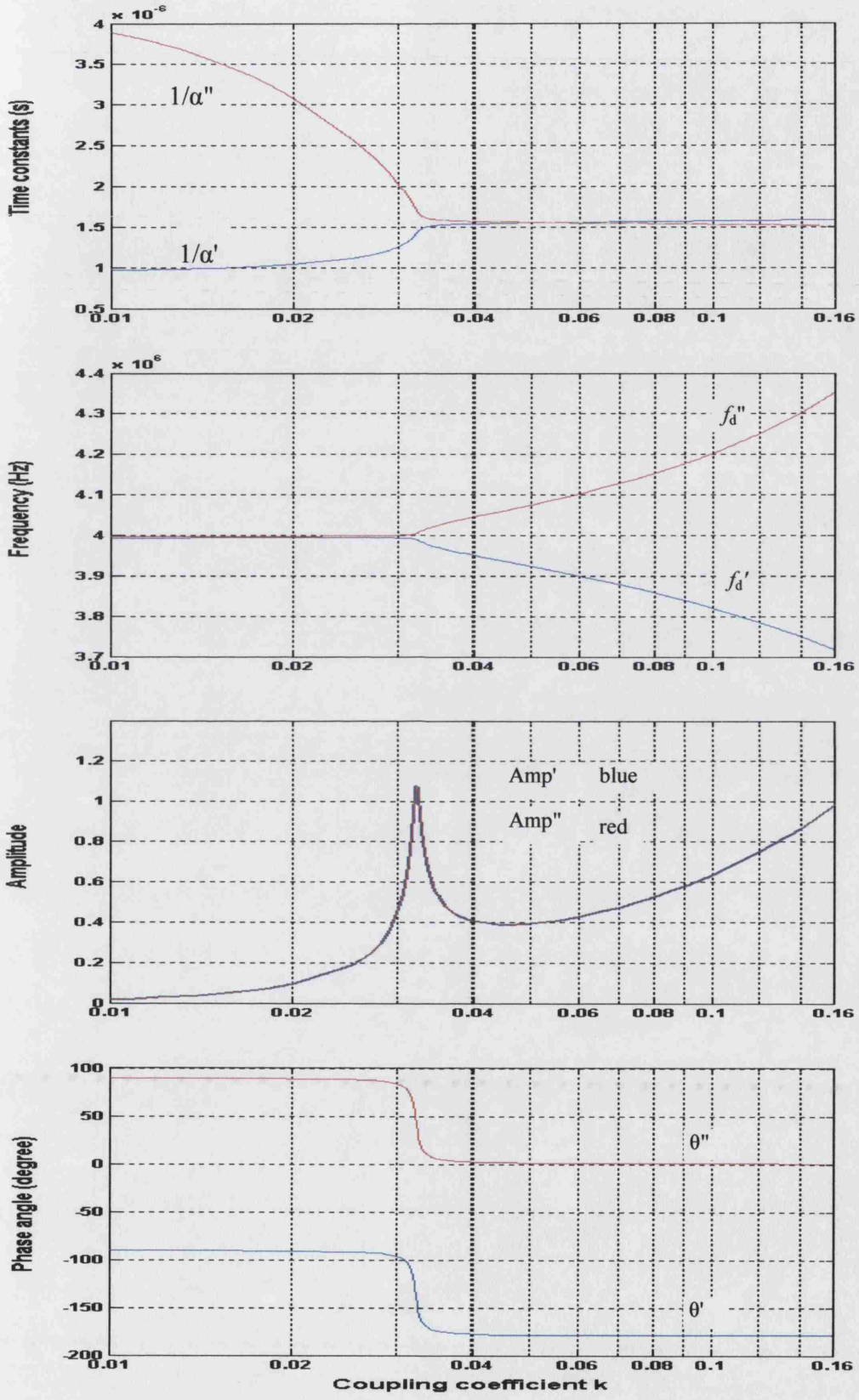


Fig.A 7.1 Verification of the analytical results.

Appendix 8 The Implant circuit

A.8.1 Implant circuit board

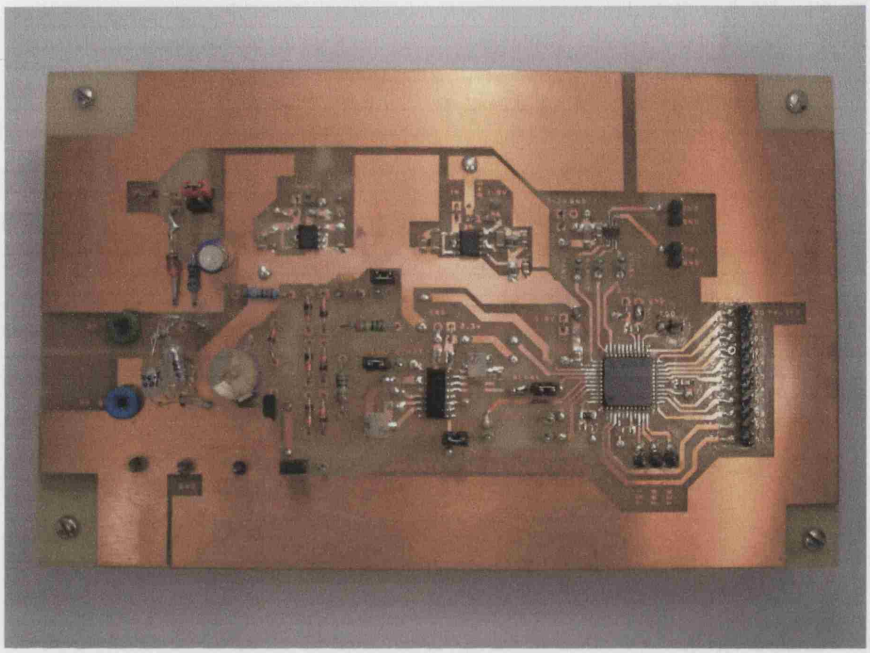


Fig.A 8.1 Picture of the implant circuit board.

A.8.2 Schematic diagram of the implant circuit

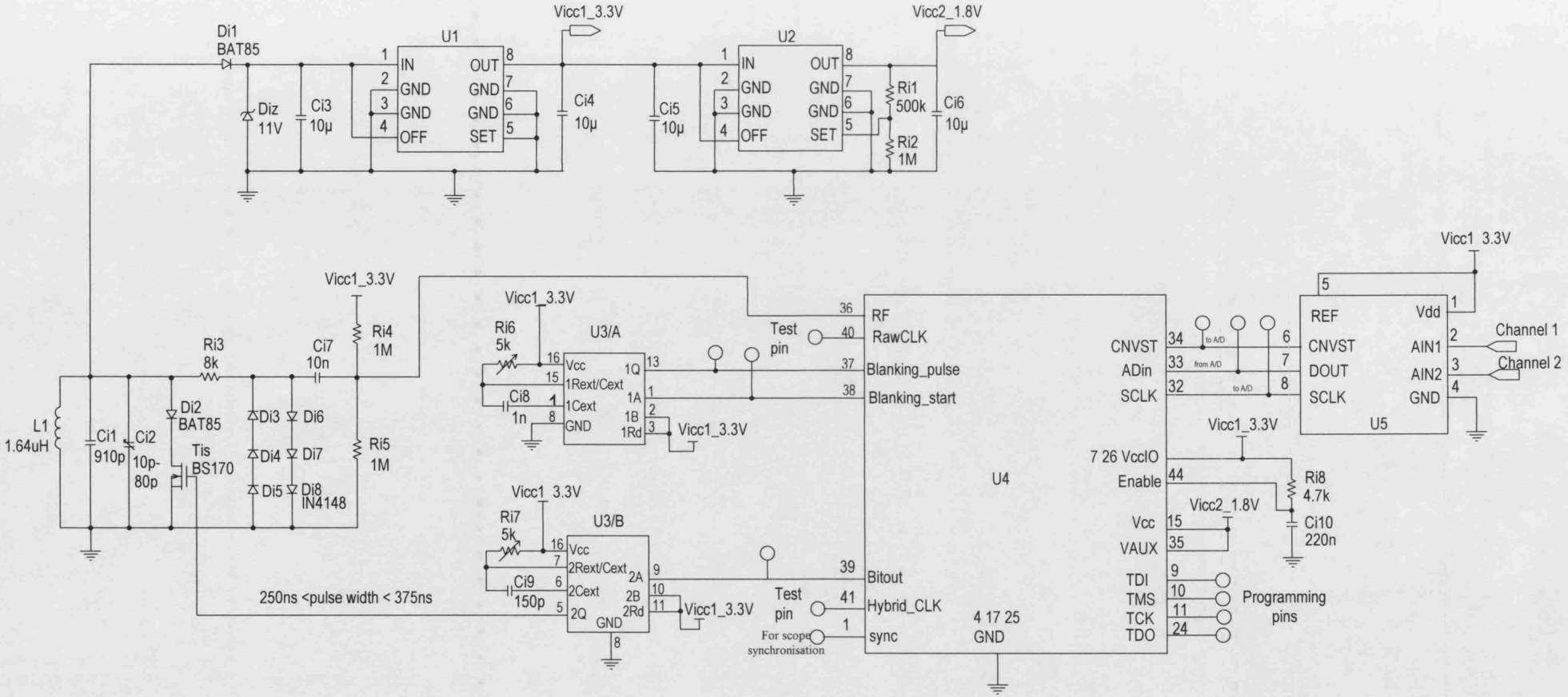


Fig.A 8.2 Schematic diagram opf the implant circuit.

Notes for the schematic diagram

1. Two voltage supplies: Vicc1_3.3V and Vicc2_1.8V.

2. ICs

IC number	Name	Maker
U1	MAX604	Maxim
U2	MAX604	Maxim
U3	74HC221	Philips Semiconductor
U4	XC2C64 VQ44	Xilinx, Inc.
U5	MAX1087	Maxim

2. Other components are L_1, $C_{i1} \sim C_{i10}$, $R_{i1} \sim R_{i8}$, $D_{i1} \sim D_{i8}$ and D_{iZ}.

3. Note for U3/A (Monostable 1): falling edge trigger, required pulse width range 2.5μs ~ 2.625μs.

Set by R_{i6} and C_{i8}, maximal pulse width $= 0.7R_{i6max}C_{i8} = 0.7 * 5k*1n = 3.5\mu s$.

4. Note for U3/B (Monostable 2): falling edge trigger, required pulse width range 250ns ~ 375ns. Maximal pulse width set by R_{i7} and $C_{i9} = 0.7R_{i7max}C_{i9} = 0.7 * 5k*150p =$ 525ns.

5. Note for U4 (the CPLD): the I/O drivers are supplied by Vicc1_+3.3V; the internal logic core is supplied by Vicc2_+1.8V.

A.8.3 VHDL file for the implant logic chip

```
--- This is the VHDL file for the logic chip in the implant circuit.
--- When powered up, signal 'enable' is from low to high, delayed and smoothed by
220nF and 4.7kΩ.
--- Radio frequency input to RF port, after a buffer, become square wave RawCLK.
--- RawCLK is to have a test pin and also used by internal logic.
--- blanking_start is to trigger the mono-stable.
--- blanking_pulse comes from the mono-stable.
--- RawCLK and Blanking_pulse ORed to make Hybrid_CLK.
--- From Hybrid_CLK, CNVST and SCLK are generated for A/D interface logic.

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
```

```
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity Imlogic is
        Port(
            enable:         in std_logic;
        ---- Hybrid_clock generation
            RF:             in std_logic;
            RawCLK:         inout std_logic;
            blanking_start:     out std_logic;
            blanking_pulse:     in std_logic;
            Hybrid_clk:         inout std_logic;
        ---- A/D interface
            cnvst:          out std_logic;
            sclk:           inout std_logic;
            Datain:         in std_logic;

            syn: out std_logic;---for synchronising the scope while testing
            bitout:out std_logic);--- bits output
end Imlogic;

architecture Behavioral of Imlogic is
        ---counters
            signal cnt1:    integer range 8 downto 0;
            signal cnt2:    integer range 21 downto 0;

        ----flag signals
            signal cnt2flag:        std_logic; --- flag for cnt2 counts once
            signal blankingflag:    std_logic; --- flag for blanking_start

        --- the 20 bits register to store the data from A/D convertor
            signal q:       std_logic_vector (19 downto 0);

        --- store the parity bit of ch1 and ch2 in P1 and P2
            signal P1:      std_logic;
            signal P2:      std_logic;

            signal load:    std_logic; --- load the bit to outbuffer
            signal outbuffer:       std_logic;
        --- enable the bit output to bitout port
            signal out_enable:      std_logic;

begin
        RawCLK <= RF;
        Hybrid_CLK <= blanking_pulse or RawCLK;

---- set up counter 1, it counts on rising edge, from 0 to 8.
process(enable,Hybrid_CLK)
```

```
begin
        if enable ='0' then
            cnt1<=0;
        elsif Hybrid_CLK = '1' and Hybrid_CLK'event then
            if cnt1 = 8 then
                cnt1<=0;
            else
                cnt1 <= cnt1 + 1;
            end if;
        end if;
end process;

--- set up operating flag
        blankingflag <= '1' when cnt1=7 else '0';
        blanking_start <= blankingflag and Hybrid_CLK;
        cnt2flag <= '1' when cnt1=0 else'0';
        load<='1' when cnt1=4 else'0';
        out_enable<=blankingflag and Hybrid_CLK;

--- set up counter 2, it counts on every cnt2flag, from 0 to 21.
process(enable,cnt2flag)
begin
        if enable ='0' then
            cnt2 <= 21;
        elsif cnt2flag = '1' and cnt2flag'event then
            if cnt2 = 21 then
                cnt2 <= 0;
            else
                cnt2 <= cnt2 + 1;
            end if;
        end if;
end process;

--- set up A/D interface signals
        cnvst <= '1' when (cnt2=0 and cnt1=8)  or (cnt2=11 and (cnt1 = 1 or
cnt1=8)) else '0';
        sclk<='1' when ((cnt2=2 or cnt2=3 or cnt2=4 or cnt2=5 or cnt2=6 or
cnt2=7 or cnt2=8 or cnt2=9 or cnt2=13 or cnt2=14 or cnt2=15 or cnt2=16 or cnt2=17 or
cnt2=18 or cnt2=19 or cnt2=20) and (cnt1=1 or cnt1=2 or cnt1=3 or cnt1=4 or cnt1=5 or
cnt1=6 or cnt1=7)) or (cnt2=10 and (cnt1=1 or cnt1=3 or cnt1=5 or cnt1=7)) or (cnt2=21
and (cnt1=1 or cnt1=3 or cnt1=5 or cnt1=7)) else '0';

--- set up synchronising signal for monitoring when testing the circuit,
--- one pulse every 22 counts on cnt2
        syn <='1' when cnt2=5 else '0';

--- read data from datain pin to internal register q
--- q(19) to q(10) for CH1, q(9) to q(0) is for CH2.
```

```
--- encoding, P1 is CH1 parity, P2 is CH2 parity.
process(enable, sclk)
begin
        if enable ='0' then
                q (19 downto 0)<= "00000000000000000000";
        elsif sclk'event and sclk ='1' then
                --- reading ch1
                if cnt2 =2 then q(19) <= datain;
                elsif cnt2=3 then q(18) <= datain;
                elsif cnt2=4 then q(17) <= datain;
                elsif cnt2=5 then q(16) <= datain;
                elsif cnt2=6 then q(15) <= datain;
                elsif cnt2=7 then q(14) <= datain;
                elsif cnt2=8 then q(13) <= datain;
                elsif cnt2=9 then q(12) <= datain;
                elsif cnt2=10  then
                        if cnt1=1 then
                                q(11) <= datain;
                        elsif cnt1=3 then
                                q(10) <= datain;
                        elsif cnt1=5 then
                                --- coding data bits for ch 1
                                P1 <= not (q(19) xor q(18) xor q(17) xor q(16) xor
q(15) xor q(14) xor q(13) xor q(12) xor q(11) xor q(10));
                        end if;
                --- reading ch2
                elsif cnt2=13 then q(9) <= datain;
                elsif cnt2=14 then q(8) <= datain;
                elsif cnt2=15 then q(7) <= datain;
                elsif cnt2=16 then q(6) <= datain;
                elsif cnt2=17 then q(5)  <= datain;
                elsif cnt2=18 then q(4)  <= datain;
                elsif cnt2=19 then q(3)  <= datain;
                elsif cnt2=20 then q(2)  <= datain;
                elsif cnt2=21 then
                        if cnt1=1 then
                                q(1) <= datain;
                        elsif cnt1=3 then
                                q(0) <= datain;
                        elsif cnt1=5 then
                                --- coding data bits for ch 2
                                P2 <= not (q(9) xor q(8) xor q(7) xor q(6) xor q(5)
xor q(4) xor q(3) xor q(2) xor q(1) xor q(0));
                        end if;
                end if;
        end if;
end process;
```

```
---loading the bit into outbuffer
process(enable, load)
begin
        if enable ='0' then
                outbuffer<='0';
        elsif load = '1' and load'event then
                if cnt2 = 4 then                        --- CH1, MSB
                        outbuffer<= q(19);
                elsif cnt2 = 5 then
                        outbuffer<= q(18);
                elsif cnt2 = 6 then
                        outbuffer<= q(17);
                elsif cnt2 = 7 then
                        outbuffer<= q(16);
                elsif cnt2 = 8 then
                        outbuffer<= q(15);
                elsif cnt2 = 9 then
                        outbuffer<= q(14);
                elsif cnt2 = 10 then
                        outbuffer<= q(13);
                elsif cnt2 = 11 then
                        outbuffer<= q(12);
                elsif cnt2 = 12 then
                        outbuffer<= q(11);
                elsif cnt2 = 13  then
                        outbuffer<= q(10);
                elsif cnt2 = 14 then
                        outbuffer<= q(9);
                elsif cnt2 = 15 then
                        outbuffer<= q(8);
                elsif cnt2 = 16 then
                        outbuffer<= q(7);
                elsif cnt2 = 17 then
                        outbuffer<= q(6);
                elsif cnt2 = 18  then
                        outbuffer<= q(5);
                elsif cnt2 = 19 then
                        outbuffer<= q(4);
                elsif cnt2 = 20 then
                        outbuffer<= q(3);
                elsif cnt2 = 21 then
                        outbuffer<= q(2);
                elsif cnt2 = 0 then
                        outbuffer<= q(1);
                elsif cnt2 = 1 then
                        outbuffer<= q(0);
                elsif cnt2 = 2 then
                        outbuffer<= P1;         -- CH1
```

```
                elsif cnt2 = 3 then
                        outbuffer<= P2;          -- CH2
                end if;
        end if;
end process;

bitout <= outbuffer and out_enable;
end Behavioral;
```

A.8.4 Implant logic pin-out

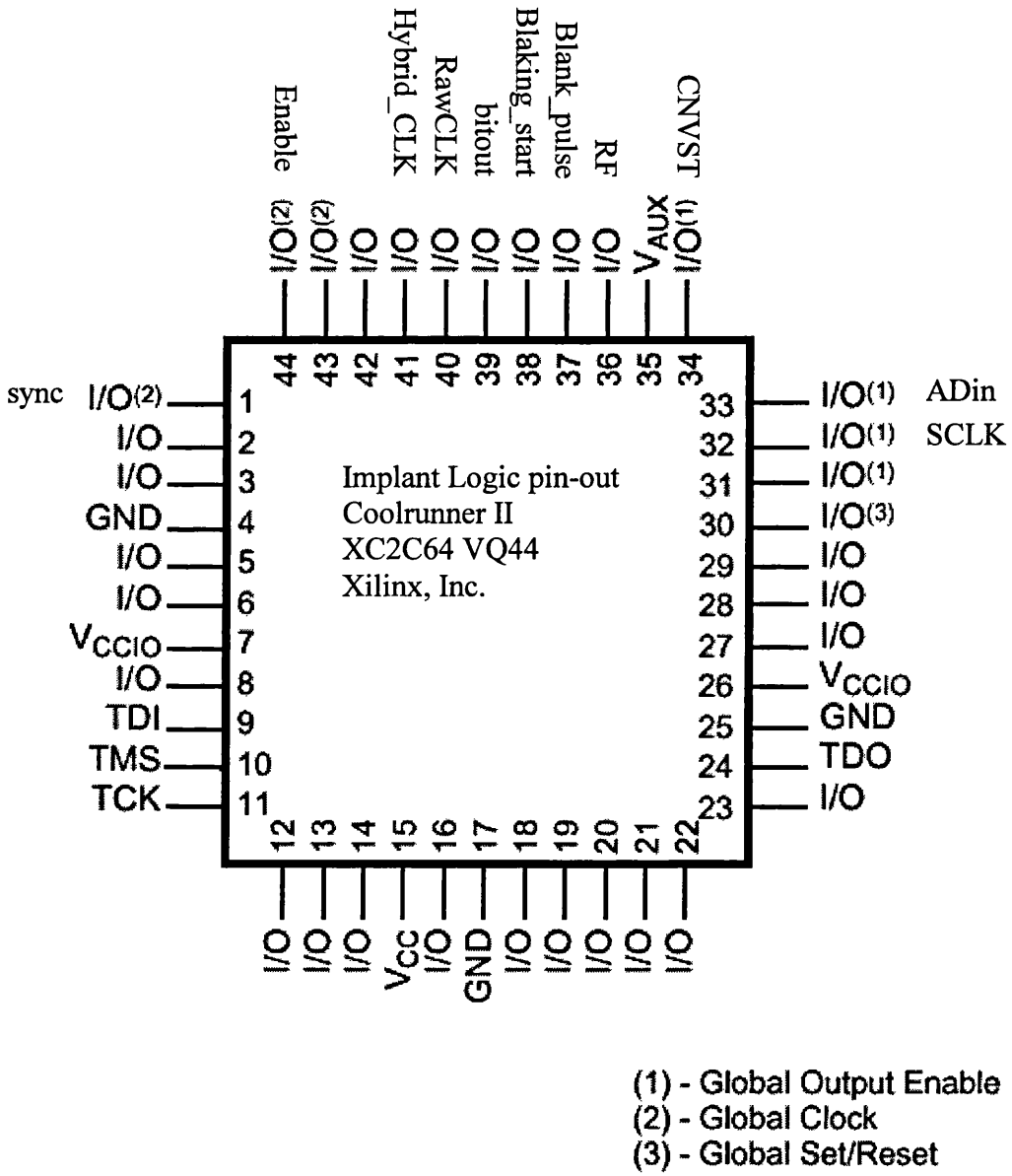


Fig.A 8.3 Implant Logic pin-out.

Appendix 9 The external circuit

A9.1 The external circuit board

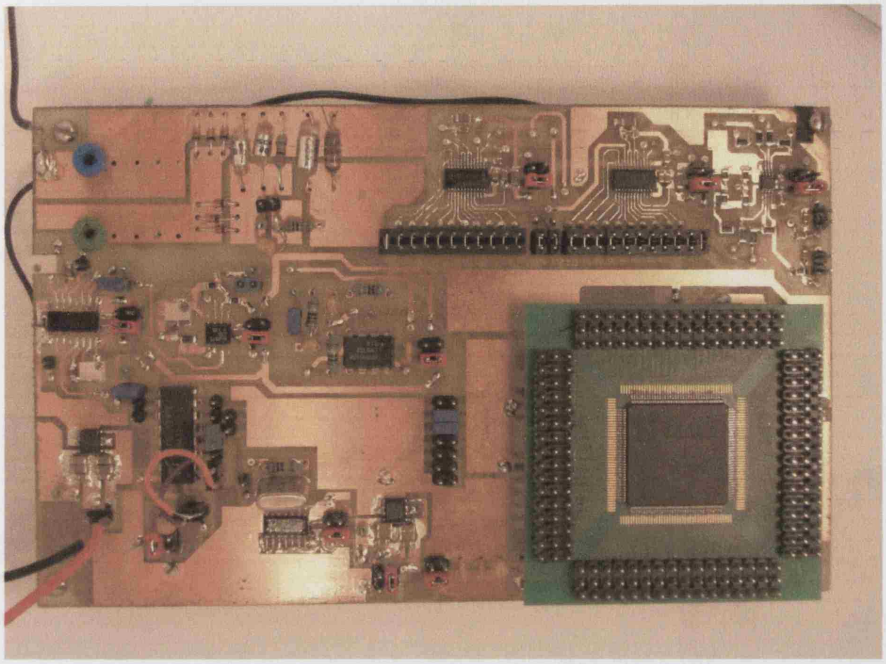
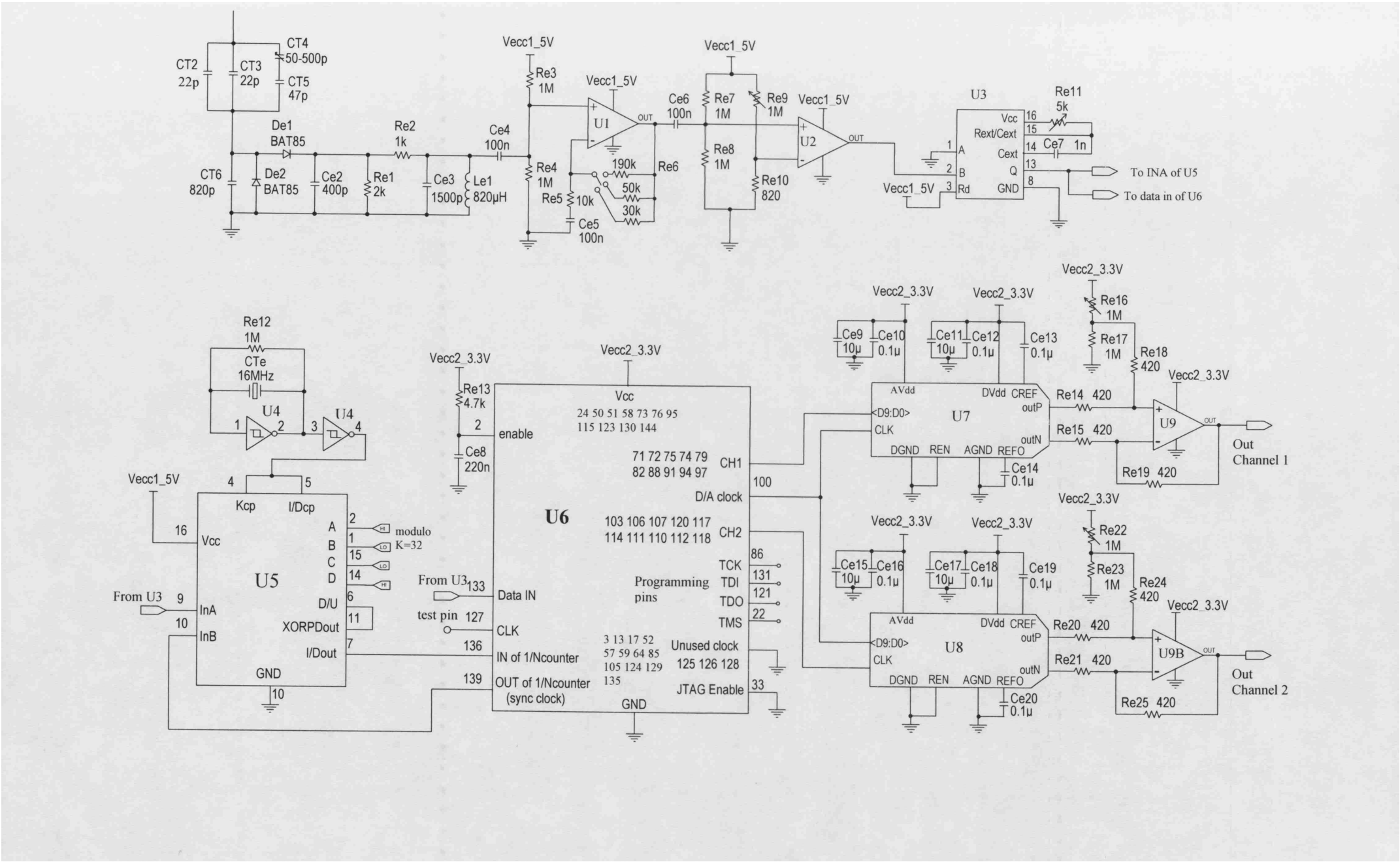


Fig.A 9.1 Picture of the external circuit board.

A9.2 Schematic diagram of the external circuit


CT2 22p
CT3 22p
CT4 50-500p
CT5 47p
CT6 820p
De1 BAT85
De2 BAT85
Re2 1k
Ce2 400p
Re1 2k
Ce3 1500p
Le1 820µH
Ce4 100n
Vecc1_5V
Re3 1M
Re4 1M
Re5 10k
Ce5 100n
U1
190k
50k
30k
Re6
Ce6 100n
Re7 1M
Re8 1M
Re9 1M
Re10 820
U2
U3
Re11 5k
Ce7 1n
Vcc
Rext/Cext
Cext
Q
GND
Rd
To INA of U5
To data in of U6
Re12 1M
CTe 16MHz
U4
Vecc2_3.3V
Re13 4.7k
Ce8 220n
enable
Vcc
24 50 51 58 73 76 95
115 123 130 144
71 72 75 74 79
82 88 91 94 97
CH1
D/A clock
100
U6
103 106 107 120 117
114 111 110 112 118
CH2
Programming pins
TCK
TDI
TDO
TMS
86
131
121
22
3 13 17 52
57 59 64 85
105 124 129
135
Unused clock
125 126 128
JTAG Enable
33
GND
Data IN
CLK
IN of 1/Ncounter
OUT of 1/Ncounter (sync clock)
From U3
test pin
U5
Kcp
I/Dcp
A
B
C
D
D/U
XORPDout
I/Dout
InA
InB
modulo K=32
U7
U8
AVdd
DVdd
CREF
outP
outN
DGND
REN
AGND
REFO
<D9:D0>
CLK
Ce9 10µ
Ce10 0.1µ
Ce11 10µ
Ce12 0.1µ
Ce13 0.1µ
Ce14 0.1µ
Ce15 10µ
Ce16 0.1µ
Ce17 10µ
Ce18 0.1µ
Ce19 0.1µ
Ce20 0.1µ
Re14 420
Re15 420
Re16 1M
Re17 1M
Re18 420
Re19 420
Re20 420
Re21 420
Re22 1M
Re23 1M
Re24 420
Re25 420
U9
U9B
Out Channel 1
Out Channel 2

Continue schematic diagram of the external circuit

Power supply

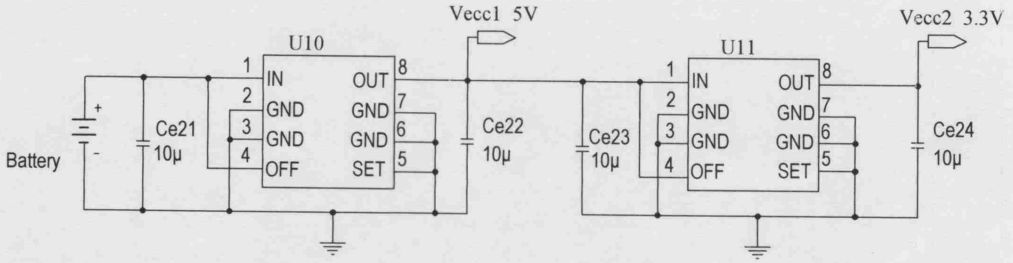


Fig.A 9.2 Schematic diagram of the external circuit.

Notes for the schematic diagram

1. Voltage supplies:
   - Vecc1_5V for U1 ~ U5
   - Vecc2_3.3V for U6 ~ U9
2. ICs in the diagram

IC number	IC name	Maker
U1	LM6132/A	National Semiconductor
U2	MAX975	Maxim Integrated Products
U3	74HC221	Philips Semiconductors
U4	74HC14	Philips
U5	74HC297	Texas Instruments
U6	XCR3384XL	Xilinx, Inc.
U7	MAX5184	Maxim
U8	MAX5184	Maxim
U9	MAX4257	Maxim
U10	MAX603	Maxim
U11	MAX604	Maxim

3. Other components include:
   - capacitors: $C_{e2} \sim C_{e24}$.
   - resistors: $R_{e1} \sim R_{e25}$.
   - diodes: $D_{e1} \sim D_{e2}$.
   - crystal resonant CT_e
4. Note for U2, other pin connections:

Pin number	Pin name	Connections
1	Vcc	Vcc
4	STAT	Vcc
5	STO	GND
6	GND	GND
8	LP	Vcc

5. Note for U3:

    - Triggered by rising edge.
    - pulse width = 0.7RC = 0.7×3.21k×1nF = 2.25μs

6. Note for U6:

- All Vcc = 3.3V, maxim 4V.
- I/O ports are 5V tolerant, maxim = 5.5V, can interface with U5 directly.
- JTAG enable (pin 33) connects to GND if JTAG programming pins are not required as I/O.

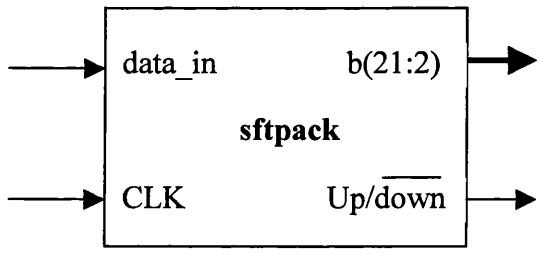
Unused pins are left unconnected, except unused CLK/IN pins which must have external termination

A9.3 VHDL files for the logic chip in the external circuit

```
--- File name: sftpack.
--- This is part 1 of the VHDL file for word synchronisation in the logic chip in the
--- external circuit.
--- It conducts sampling, parity checking, comparison and generating a up/down signal.
--- When power up, 'enable' is from low to high, delayed and smoothed by 220nF and --
-- 4.7kΩ.

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity sftpack is
        Port (
        data_in:    in std_logic;
        CLK:        inout std_logic;
                    --- invert of the sync_clock from PLL output.
        b:          out std_logic_vector (21 downto 2); -- parallel data from
                    --- the shift register
        up_down:    out std_logic);
end sftpack;

architecture Behavioral of sftpack is
        signal q:   std_logic_vector (21 downto 0);     buffer in the shift
                    --- register
        check1:     std_logic; --- parity check result for b21 ~ b12
        check2:     std_logic: --- parity check result for b11 ~b2

begin

--- input a data bit into the shift register
```

```
process (CLK)
begin
        if (CLK'event and CLK='1') then      --- sample at rising edge of CLK.
            q <= q(20 downto 0) & data_in;
        end if;
end process;

        b(21 downto 2) <= q(21 downto 2);
        check1 <=not((q(12) xor q(13)) xor (q(14) xor q(15)) xor (q(16) xor
q(17))xor (q(18) xor q(19)) xor (q(20) xor q(21)));
        check2 <=not((q(2) xor q(3)) xor (q(4) xor q(5)) xor (q(6) xor q(7)) xor
(q(8) xor q(9)) xor (q(10) xor q(11)));
        up_down <= (q(0) xor check2) or (q(1) xor check1);
end Behavioral;
```

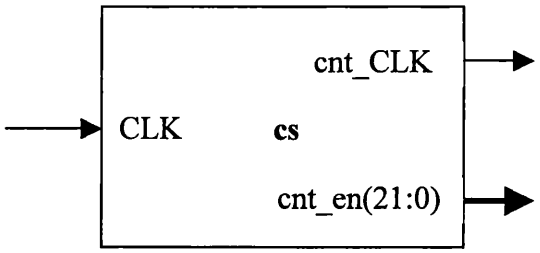
Symbol generated from the file



```
--- File name: cs.
--- This is part 2 of the VHDL file for word synchronisation in the logic chip in the
--- external circuit.
--- It is for selecting an active counter

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity cs is
        port(
        CLK:        inout std_logic;
        cnt_CLK:    out std_logic; --- invert of CLK. For sampling up_down
                    --- signal at falling edge of the CLK.
        cnt_en:     out std_logic_vector (21 downto 0));
end cs;

architecture Behavioral of cs is

begin

----- enable one counter at a rising edge of CLK. Total 22 cnt_en lines.
process (CLK)
        variable count: integer range 0 to 21;
begin
        if (CLK'event and CLK='1') then
            --- reset all cnt_ens to 0.
            cnt_en(21 downto 0)<="0000000000000000000000";
                if count >= 21 then
                        count := 0;
                else
                        count := count+1;
```

```
                    end if;

                    case count is
                        when 0 =>     cnt_en(0) <= '1';
                        when 1 =>     cnt_en(1) <= '1';
                        when 2 =>     cnt_en(2) <= '1';
                        when 3 =>     cnt_en(3) <= '1';
                        when 4 =>     cnt_en(4) <= '1';
                        when 5 =>     cnt_en(5) <= '1';
                        when 6 =>     cnt_en(6) <= '1';
                        when 7 =>     cnt_en(7) <= '1';
                        when 8 =>     cnt_en(8) <= '1';
                        when 9 =>     cnt_en(9) <= '1';
                        when 10=>     cnt_en(10) <= '1';
                        when 11=>     cnt_en(11) <= '1';
                        when 12=>     cnt_en(12) <= '1';
                        when 13=>     cnt_en(13) <= '1';
                        when 14=>     cnt_en(14) <= '1';
                        when 15=>     cnt_en(15) <= '1';
                        when 16=>     cnt_en(16) <= '1';
                        when 17=>     cnt_en(17) <= '1';
                        when 18=>     cnt_en(18) <= '1';
                        when 19=>     cnt_en(19) <= '1';
                        when 20=>     cnt_en(20) <= '1';
                        when 21=>     cnt_en(21) <= '1';
                    end case;
            end if;
end process;

            cnt_CLK<= not(CLK); ---generating a clock in order to use the falling
            --- edge of the CLK.


end Behavioral;
```

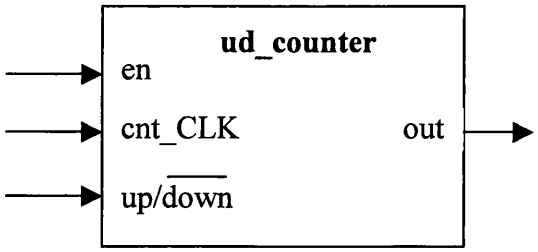
Symbol generated from the file



```
--- File name: ud_counter.
--- This is part 3 of the VHDL file for word synchronisation in the logic chip in the
--- external circuit.
--- It is for operating the up/down counters.

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity ud_counter is
        Port (
        en:         in std_logic;   --- connect to corresponding cnt_en (x)
                                    --- from cs.vhd.
        cnt_CLK:    in std_logic;   --- connect to cnt_CLK from cs.vhd.
        up_down:    in std_logic;   --- connect to up_down from sftpack.vhd.
        out:        out std_logic);         --- output after comparing to the
                                            --- threshold.
end ud_counter;

architecture Behavioral of ud_counter is
begin
process (clk,enable)
        variable cnt_number: integer range 0 to 20; --- store the counts
begin
        if (en='0') then
                out <= '0';     --- if the counter is not selected, output 0.
        elsif (cnt_CLK 'event and cnt_CLK='1') then
                if up_down = '1' then   --- count up
                        if cnt_number >= 20 then
                                cnt_number:=16;     --- cap the counts below 20
                                                    --- but above the threshold.
```

```
                    else
                        cnt_number:=cnt_number+1; --- n = 1.
                    end if;
                elsif up_down='0' then          --- count down
                    if cnt_number <=2 or cnt_number >= 30 then
                        cnt_number:=4; --- keep the counts above 4.
                    else
                        cnt_number:=cnt_number-2; --- m=2
                    end if;
                end if;

                if cnt_number >= 16 and cnt_number <=20 then
                    out<= '1';      --- output high if exceed threshold '16'.
                else
                    out <= '0';     --- output low if less than threshold.
                end if;
            end if;

end process;
end Behavioral;
```

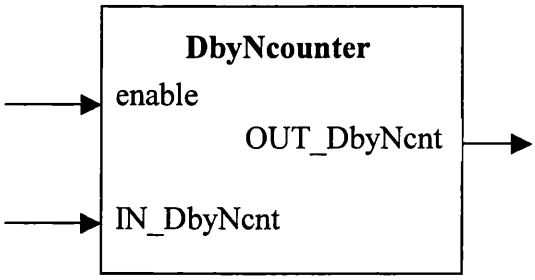
Symbol generated from the file



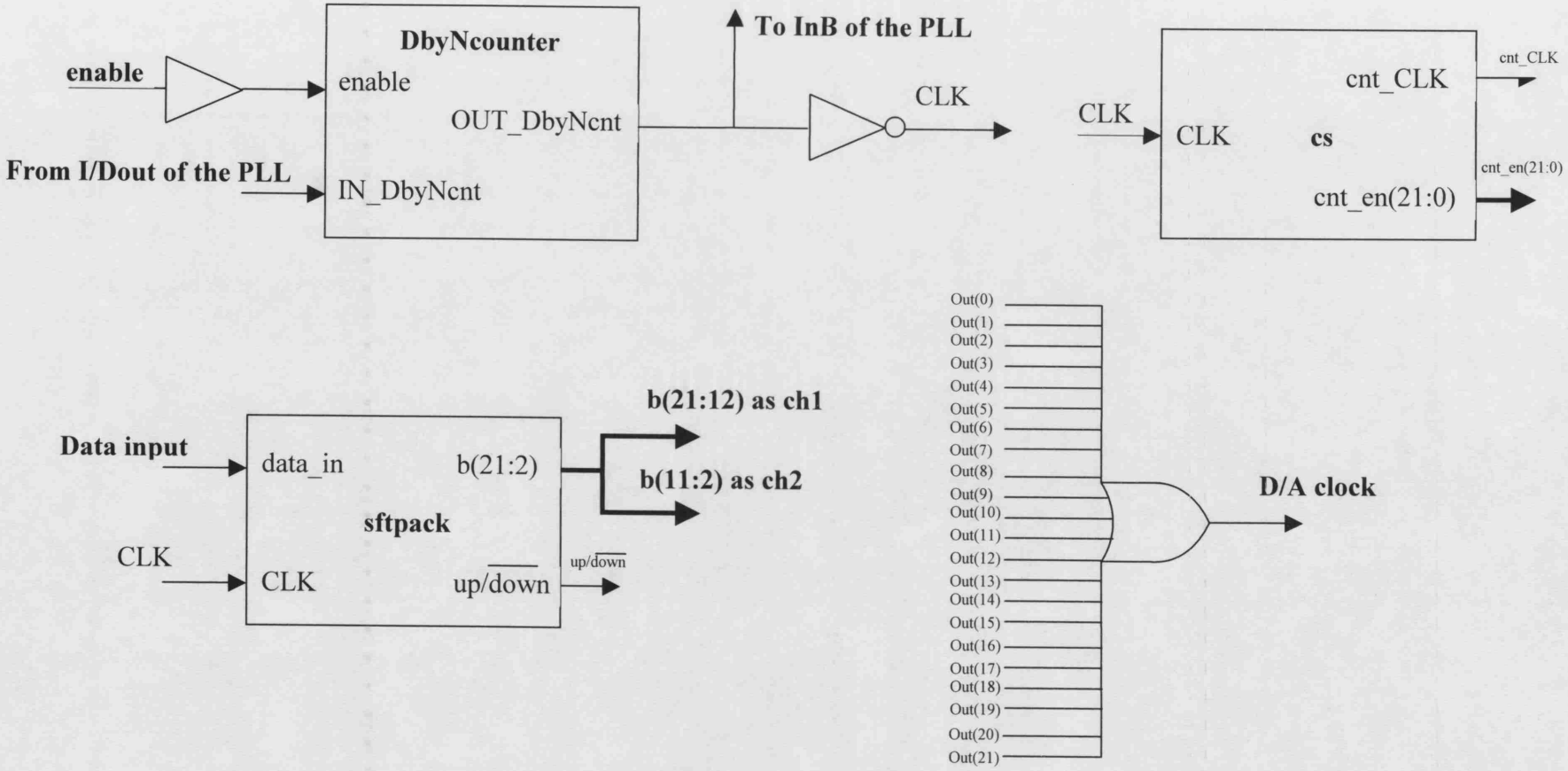
```
--- File name: DbyNcounter.
--- This program is to generate a divided by N counter for the bit synchronisation,
--- to work with PLL.
--- Inputs are: enable, IN_DbyNcnt connecting to PLL I/Dout pin 7.
--- In/output is: OUT_DbyNcnt connecting to PLL feedback inputB, pin 10 and
internally connecting to the input of an inverter to generate CLK which is the master
clock for word synchronisation.

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity DbyNcounter is
        Port(
        enable:         in std_logic;
        IN_DbyNcnt:     in std_logic;
        OUT_DbyNcnt:    inout std_logic);
end DbyNcounter;

architecture Behavioral of DbyNcounter is
begin
process (DbyNcntin, enable)
        variable DbyNcount: integer range 0 to 36;   ---
begin
        if enable ='1' then
                DbyNcount :=0;
        elsif IN_DbyNcnt ='1' and IN_DbyNcnt'event then
                if DbyNcount >= 36 then
                        DbyNcount:=0;
                        OUT_DbyNcnt <= not (OUT_DbyNcnt);
                else
```

```
                    DbyNcount := DbyNcount +1;
                end if;
            end if;
end process;
end Behavioral;
```

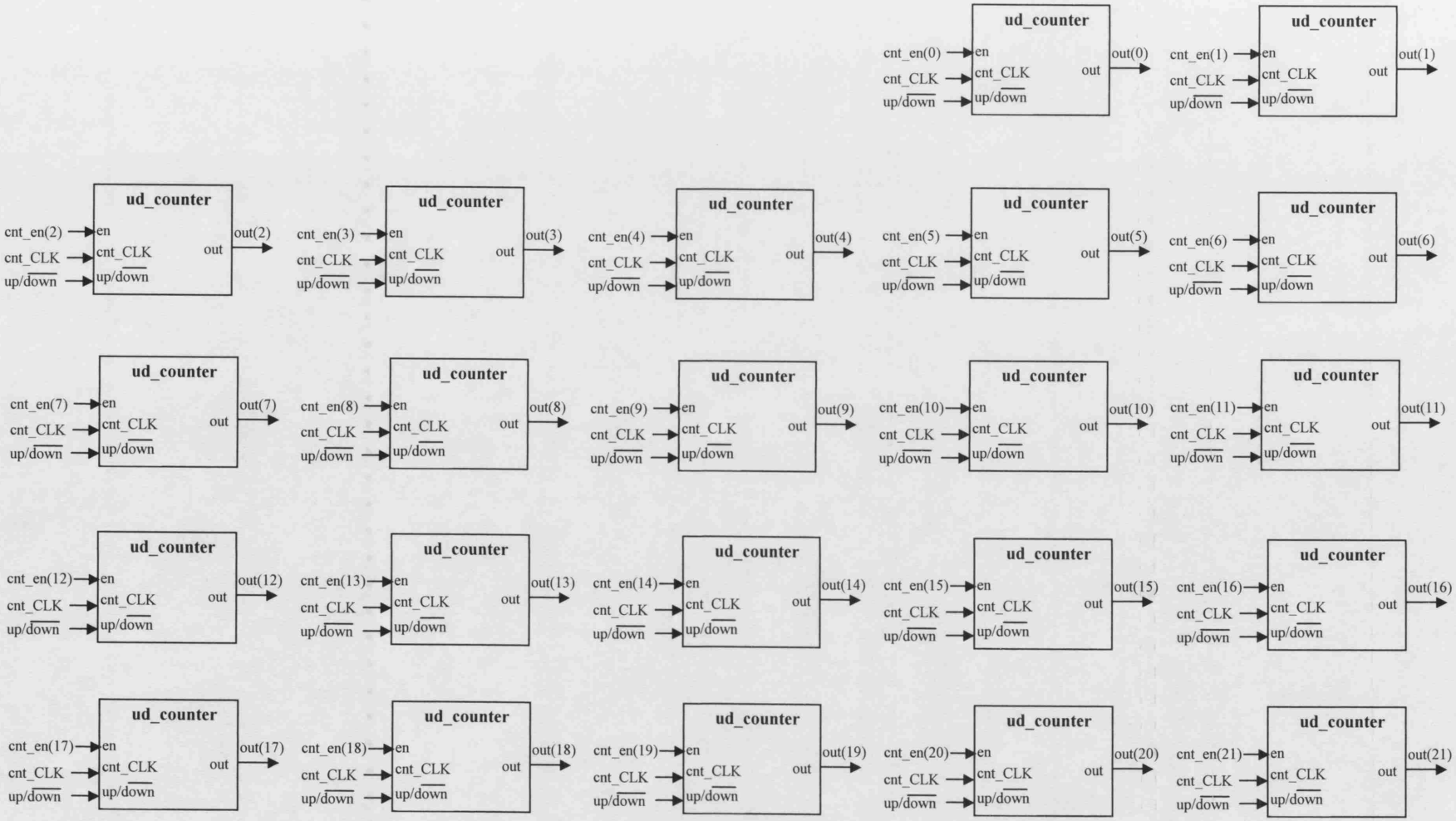
Symbol generated from the file



--- File name: Top./part 1



--- File name: Top/part2



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